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A MEMS Sensors Based on A Laterally Movable Gate Field-Effect Transistor (LMGFET) with A Novel Decoupling Sandwich Structure

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ABSTRACT

This paper presents the development of a novel micro force sensor based on a laterally movable gate field-effect transistor (LMGFET). A precise electrical model is proposed for the performance evaluation of small-scale LMGFET devices and exhibits improved accuracy in comparison with previous models. A novel sandwich structure consisting of a gold cross-axis decoupling gate array layer and two soft photoresistive SU-8 layers is utilized. With the proposed dual-differential sensing configuration, the output current of the LMGFET lateral operation under vertical interference is largely eliminated, and the relative output error of the proposed sensor decreases from 4.53% (traditional differential configuration) to 0.01%. A practicable fabrication process is also developed and simulated for the proposed sensor. The proposed LMGFET-based force sensor exhibits a sensitivity of 4.65 $\mu A \cdot nN^{-1}$, which is comparable with vertically movable gate field-effect transistor (VMGFET) devices, but has an improved nonlinearity of 0.78% and a larger measurement range of ±5.10 μN. These analyses provide a comprehensive design optimization of the electrical and structural parameters of LMGFET devices and demonstrate the proposed sensor's excellent force-sensing potential for biomedical micromanipulation applications.

1. Introduction

Micro-electromechanical system (MEMS) micro force sensors are efficient and necessary tools in many biomedical studies. Such tools have been used to measure the Young's modulus [1,2], viscosity [3,4], and locomotion traction [5] in living cells or tissues in order to study biological processes and biomedical reactions. Micro force sensors can provide precise force feedback in micro-robotic biomedical manipulations to improve the automation extent [6,7] and the survival rate of biological objects [8,9]. Recent studies have focused on the organelle or molecular level, thereby increasing the demand for ultralow force sensing below the nanonewton level. Current force-sensing devices are mainly based on sensing principles, such as capacitive [10,11], piezoresistive [12,13], and piezoelectric [14,15] principles. The movable gate field-effect transistor (MGFET) force sensor exhibits several advantages over its competitors, such as a high sensitivity derived from the transistor array design [16,17], convenient signal amplification, and modulation with integrated circuits [18], thus making the on-chip measurement of low-scale forces feasible. Compared with traditional metal-oxide semiconductor field-effect transistors, MGFET devices have a floating gate over the substrate channel area and can move along three axes due to the air gap, as shown in Fig. 1. The current

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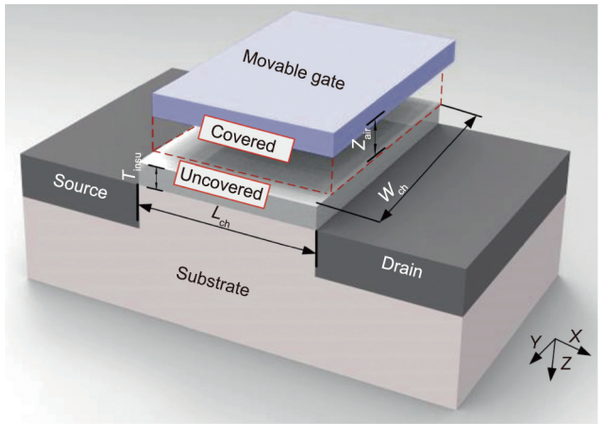

Fig. 1. Sensing unit of the MGFET. T_{insu}: insulator thickness; L_{ch}: channel length; Z_{air}: air gap thickness; W_{ch}: whole channel width.

between the source and the drain electrodes reflects the applied external loads. In terms of the gate moving direction, MGFET devices are divided into two types: vertically MGFETs (VMGFETs) and laterally MGFETs (LMGFETs). VMGFETs exhibit high sensitivity, while their movement range is limited by the small air gap thickness. Their measurement linearity deteriorates with an increase in gate vertical deformation. Unexpected rapidly increased loads usually occur during biomedical measurements, such as during membrane penetration in biological cell microinjections [19,20], when the force amplitude increases sharply and may exceed the measurement range of a VMGFET device. In LMGFETs, the gate moves laterally along the channel width, and the air gap remains constant. The measurement range of LMGFETs is larger than that of VMGFETs, and their output current changes linearly during the measurement range. Therefore, a highly sensitive LMGFET force sensor is more versatile than a VMGFET in biomedical measurement.

Researchers have developed several MGFET devices on the basis of these two types, such as VMGFET-based accelerometers [21,22], differential amplifiers [23], and LMGFET-based displacement sensors [24]. Existing studies have found that the measuring sensitivity can be improved by scaling down the transistor size. However, the widely adopted long-channel model in Refs. [21–24], which ignores many scale effects, is inaccurate for describing MGFET performance, especially for devices with a small size. In our previous work, we proposed an accurate electrical model for small-scale VMGFET devices [25]. However, the movable gate of an LMGFET device partially covers the channel area, leaving the other part exposed. The operation behavior of LMGFET devices is relatively more complex than that of VMGFET devices, such that the previous VMGFET model is no longer applicable in LMGFET design. Therefore, a new precise electrical model is essential for the performance evaluation of small LMGFET devices. Moreover, the output current of an MGFET changes as its gate moves laterally and vertically, and loads from non-operation directions can produce considerable interference of output signals.

A differential sensing configuration has usually been adopted to attenuate the cross-axis coupling effect in MGFET devices [23,25]. However, this method is invalid for LMGFETs because the output current changes significantly when the gate moves vertically. The output change from lateral loads can be overwhelmed by vertical disturbances, producing undesirable measurement errors. Therefore, a novel decoupling movable structure and sensing configuration is required to improve sensing accuracy. The measuring sensitivity of MGFET devices can be further improved by lowering the stiffness of movable structures. In existing MGFET devices, movable structures are made of rigid materials, such as silicon [21] and nickel [22,24] with large stiffness, such that the movable structure can hardly deform. One feasible method to improve the measuring sensitivity is to replace these stiff materials with other flexible alternatives. However, this is difficult for LMGFET devices, as they require high-aspect-ratio structures, and no such attempts have been conducted before.

The main contributions of this work are as follows. First, a separated channel-based electrical model is proposed to describe the operation behavior of small LMGFET devices, and its improved accuracy and capability for performance evaluation are demonstrated. Second, the electrical and structural parameters of LMGFET devices are fully analyzed to optimize the performance of ultralow force-sensing applications. Third, a flexible sandwich structure is proposed for the LMGFET micro force sensor, which consists of a gold cross-axis decoupling gate array layer and two soft photoresistive SU-8 layers. The sensor utilizes a novel dual-differential decoupling sensing configuration that exhibits excellent sensing sensitivity and anti-interference capability. Finally, the proposed LMGFET force sensor is simulated with a practicable fabrication process. The proposed sensor breaks through the limitation between the sensing accuracy and measurement range of MGFET devices. Its measuring sensitivity is 4.65 $\mu A \cdot nN^{-1}$ for a large measurement range of ±5.10 μN, and its nonlinearity is less than 0.78%.

The rest of this paper is organized as follows: Section 2 models and analyzes the electrical behavior of the LMGFET. Section 3 illustrates the proposed LMGFET force sensor and describes the mechanical model and sensing configuration. Section 4 presents a practicable fabrication process for the proposed sensor. The theoretical model is then validated through simulation and experimental results, followed by a discussion of the sensor performance. Section 5 provides the conclusions.

2. Electrical modeling of the LMGFET

When the gate of an LMGFET moves laterally, the channel width changes such that the LMGFET can be divided into two separated parts—namely, a covered channel area with width W_{chc} and an uncovered channel area with width W_{chu} ($W_{chu} = W_{ch} - W_{chc}$) (where W_{ch} is the whole channel width). The two parts share some common parameters, such as the channel length L_{ch}, voltage difference between the gate and source electrode V_{gs}, and voltage difference between the drain and source electrode V_{ds}. Due to the difference in the gate modulation effect at different lateral positions, the electron conductance in each channel area differs significantly. The whole channel exhibits several individual electrical parameters, such as the gate capacitance C'_{eff}, carrier mobility U'_{eff}, and channel current I_{ds}. Thus, an investigation of the electrical parameters in each part is necessary in order to understand the operation principles of the LMGFET. Such an investigation is conducted in this section.

2.1. Effective gate capacitance

The capacitance between the gate and the covered and uncovered channel area changes when the gate moves laterally. Gate capacitance is a parameter describing the capacitance over a unit area. More specifically, the effective gate capacitance in the covered channel area C'_{effc} is the series capacitance of the air gap and gate insulator, which can be expressed as follows:

$$C'_{effc} = \frac{\varepsilon_0}{\frac{\varepsilon_0 T_{insu}}{\varepsilon_{insu}} + Z_{air}} = \frac{\varepsilon_0}{Z'_{effc}} \tag{1}$$

where $\varepsilon_0 = 8.854 \times 10^{-14}$ F·cm^{-1} is the permittivity of air; ε_{insu} is the permittivity of the insulator; Z_{air} is the air gap thickness; T_{insu}

is the insulator thickness; and Z'_{effc} is the effective gate gap thickness in the covered area. A previous study assumed that the effective gate capacitance in the uncovered channel area C'_{effu} is constant during gate movement [24]; however, this assumption is not in accordance with reality and can cause many artifacts in the device performance estimation. In this study, we propose an accurate variable expression of C'_{effu} based on the fringe parasitic effect of the gate sidewall and bottom line [26,27]:

$$C'_{effu} = \frac{2\varepsilon_0}{\pi W_{chu}} \ln\left[\frac{Z'_{effc} + T'_g + \sqrt{T'^2_g + 2T'_g Z'_{effc}}}{Z'_{effc}}\right] + \frac{k\varepsilon_0}{\pi W_{chu} L_{ch}} \ln\left[\frac{\pi L_{ch}}{Z'_{effc}}\right] = \frac{\varepsilon_0}{Z'_{effu}} \tag{2}$$

where $T'_g = T_g e^{\left(\frac{\pi W_{chu} - \sqrt{T_g^2 + 2T_g Z'_{effc}}}{\beta Z'_{effc}}\right)}$ is the effective gate thickness for the sidewall parasitic capacitance; T_g is the gate thickness; k and β are fitting parameters; and Z'_{effu} is the effective gate gap thickness in the uncovered area.

The effective gate capacitance of the two separated areas is examined at different lateral and height positions and compared with simulation results from the finite-element method (FEM) software Ansoft Maxwell. In this calculation, the whole channel width W_{ch} is 20 μm; the air gap thickness Z_{air} is from 0.1 to 0.5 μm; the gate thickness T_g is 0.2 μm; the gate insulator is silicon nitride, and its thickness T_{insu} is 100 nm; and the channel length L_{ch} is 5 μm. During gate movement, most of the electric potential is concentrated in the covered area, and a small amount is scattered on the boundary edge because of the fringe parasitic effect. The effective gate capacitance in the covered channel area C'_{effc} remains almost constant at full width. As the covered area width W_{chc} approaches zero, the scattered potential proportion increases, and C'_{effc} experiences a small increase, as shown by the dots in Fig. 2. However, the relative error of C'_{effc} between the model and the simulation results is less than 3.0% for a small W_{chc} of 1 μm in three different air gaps. The value of the effective gate capacitance in the uncovered channel area C'_{effu} is one order less than that of C'_{effc}. The gate capacitance in the uncovered area mainly results from the scattered electric potential in the gate sidewall and bottom line. The total electrical potential remains constant, but the size of the uncovered area changes during gate movement. C'_{effu} exhibits an inversely proportional relationship with width in the covered area W_{chc}. When W_{chc} is low, C'_{effu} increases slowly because the change in W_{chu} is insignificant. However, the size of the uncovered area changes greatly as W_{chc} approaches the whole channel width, resulting in a rapid increase of C'_{effu}. The scattered electrical potential increases as the air gap Z_{air} decreases and then aggravates this phenomenon. The calculation of C'_{effu} also shows an excellent coincidence with the simulated results, where the largest relative error is less than 3.5%.

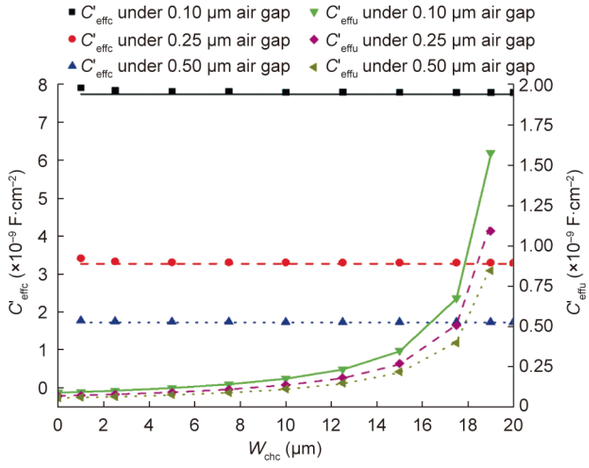

Fig. 2. Relationship between the effective gate capacitances C'_{effc} and C'_{effu}, and the channel width at different air gaps. Lines represent the calculated capacitance, while scatters are the simulated results.

2.2. Threshold voltage

Threshold voltage is a crucial switch parameter modulating the current channel between the source and drain electrodes. The channel current exists only if the gate voltage is larger than the threshold voltage for an accumulation-type MGFET. For a depletion-type device, in which the channel current is originally induced, a gate voltage approaching the threshold value can break off the conducting channel. The covered and uncovered channel areas have different threshold voltages, so they can have different channel statuses during lateral and vertical gate movement. Considering the short and narrow channel effects, the threshold voltages in the two areas are modeled separately, as follows:

$$V_{thc} = \varphi_{MS} + \varphi_B \pm F_S \frac{Z'_{effc}\sqrt{|2qN_{a/d}\varepsilon_{si}(\varphi_B - V_{bs})|}}{\varepsilon_0} \mp \frac{Q'_{eff} Z'_{effc}}{\varepsilon_0} + F_{Nc}(\varphi_B - V_{bs}) \tag{3}$$

$$V_{thu} = \varphi_{MS} + \varphi_B \pm F_S \frac{Z'_{effu}\sqrt{|2qN_{a/d}\varepsilon_{si}(\varphi_B - V_{bs})|}}{\varepsilon_0} \mp \frac{Q'_{eff} Z'_{effu}}{\varepsilon_0} + F_{Nu}(\varphi_B - V_{bs}) \tag{4}$$

where φ_{MS} is the work function difference between the gate and channel; φ_B is the channel built-in voltage, which is $\frac{k_B T}{q}\ln\left(\frac{N_a}{n_i^2}\right)$ and $-\frac{k_B T}{q}\ln\left(\frac{N_d}{n_i^2}\right)$ for an N-channel device and a P-channel device, respectively; $N_{a/d}$ is the net concentration of ionized acceptors in a P-type substrate and donors in an N-type substrate, respectively; $q = 1.6 \times 10^{-19}$ C is the magnitude of the electron or hole charge, n_i is the intrinsic doping concentration of silicon, k_B is the Boltzmann constant, and T is the thermodynamic temperature; ε_{si} is the permittivity of silicon; V_{bs} is the voltage difference between the source and substrate electrodes; Q'_{eff} is the effective charge density of the channel, where the minus and plus signs are respectively for N-channel and P-channel devices; and F_S is the channel length coefficient, which is expressed as follows:

$$F_S = 1 - \frac{X_j\left[a + d_0 + d_1\frac{\sqrt{\frac{|2\varepsilon_{si}(\varphi_B - V_{bs})|}{qN_a}}}{X_j} + d_2\left(\frac{\sqrt{\frac{|2\varepsilon_{si}(\varphi_B - V_{bs})|}{qN_a}}}{X_j}\right)^2\right]}{L_{ch}} \times \sqrt{1 - \left(\frac{\sqrt{\frac{|2\varepsilon_{si}(\varphi_B - V_{bs})|}{qN_a}}}{X_j + \sqrt{\frac{|2\varepsilon_{si}(\varphi_B - V_{bs})|}{qN_a}}}\right)^2} - \frac{aX_j}{L_{ch}} \tag{5}$$

where X_j is the depth of the P—N junctions in the source or the drain electrode; and a, d_0, d_1, and d_2 are model parameters. F_{Nc} and F_{Nu} are the channel width coefficients in the covered and uncovered channel areas, respectively, and are expressed as follows:

$$F_{Nc} = \frac{\delta\pi\varepsilon_{si} Z'_{effc}}{4W_{chc}\varepsilon_0} \tag{6}$$

$$F_{Nu} = \frac{\delta \pi \varepsilon_{si} Z'_{effu}}{4 W_{chu} \varepsilon_0} \quad (7)$$

where δ is the channel width model factor. The positive sign before the F_S term is for an N-channel device while negative sign is for a P-channel device. The sign before the Q'_{eff} term is opposite compared with that before the F_S term, and the difference between the F_S and the Q'_{eff} term can primarily determine the value of the threshold voltage. For example, a large Q'_{eff} term can result in a negative threshold voltage for a depletion-type MGFET device with a P-type substrate (Fig. 3).

Although the channel length coefficient F_S remains constant, the channel width coefficient changes during lateral and vertical gate movements, especially for the uncovered channel area, whose effective gate gap Z'_{effu} varies significantly at different positions. Therefore, the threshold voltage will exhibit different characteristics in the two channel areas and needs comprehensive analysis. The effective charge density of the channel Q'_{eff} and the substrate concentration $N_{a/d}$ are studied first. A P-type substrate device is adopted as an example, with the following parameters: The channel width W_{ch} is 20 μm, the air gap Z_{air} is 0.25 μm, the channel length L_{ch} is 5 μm, the P–N junction depth X_j is 0.5 μm, the intrinsic doping concentration n_i is 1.5×10^{10} cm^{-3}, the implanted model constant a = 0.04, d_0 = 0.0631353, d_1 = 0.8013292, d_2 = 0.01110777, the work function voltage difference φ_{MS} = 3.83 V, and the voltage difference between the substrate and the source electrode V_{bs} = 0 V. The remaining parameters are the same as those given in Section 2.1. The effect of the substrate acceptor concentration N_a is investigated from Case_1 to Case_4 in Table 1, where N_a increases from 5×10^{14} to 5×10^{15} cm^{-3}, while Q'_{eff} is kept low at 2.5×10^{-8} C·cm^{-2}. For a small N_a in Case_1, both parts behave as depletion-type transistors, and the channel is initially conductive because their energy band has been bent by dominant electrons in the channel surface. To break off the conducting channel, a negative threshold voltage is required to attract holes in the substrate. However, V_{thc} becomes positive while V_{thu} remains negative when N_a increases to 1.0×10^{15} cm^{-3}; the covered part becomes an accumulation-type transistor, and the uncovered part remains a depletion type in Case_2. Because of its flat energy band, the channel in the covered area is not conductive until the inversion layer is formed, wherein holes gather in the channel surface under electrical potential forces resulting from a positive threshold voltage V_{thc}. This condition appears to be desirable for device design, because the uncovered part with a nonlinear effective gate capacitance can be eliminated. However, it results in poor device performance, as only the covered part contributes to the output current.

Table 1
Threshold voltage of covered/uncovered channel area under different electrical parameters.

Case	N_a (cm^{-3})	Q'_{eff}(C·cm^{-2})	V_{thc} (V)[a]	V_{thu} (V)[b]
1	5×10^{14}	2.5×10^{-8}	–	–
2	1×10^{15}	2.5×10^{-8}	+	–
3	3×10^{15}	2.5×10^{-8}	+	–/+
4	5×10^{15}	2.5×10^{-8}	+	+
5	1×10^{15}	1.0×10^{-8}	+	–
6	1×10^{15}	5.0×10^{-8}	–	–
7	1×10^{15}	1.0×10^{-7}	–	–
8	1×10^{15}	3.0×10^{-7}	–	–

[a] "+" and "–" refer to accumulation and depletion types, respectively.
[b] "–/+" indicates that the device changes from a depletion to accumulation type.

During LMGFET operation, V_{thc} decreases moderately and V_{thu} increases sharply as W_{chc} increases, indicating that V_{thu} is more susceptible to channel width modulation. More specifically, V_{thu} changes from −0.817 V at a W_{chc} of 13 μm to 0.074 V at a W_{chc} of 14 μm in Case_3. This condition can make the uncovered area change from a depletion type to an accumulation type during operation and should be avoided. When N_a increases above 5×10^{15} cm^{-3}, the two areas become accumulation types in Case_4. The effect of the channel's effective charge density Q'_{eff} is then investigated from Case_5 to Case_8, where Q'_{eff} increases from 1×10^{-8} to 3×10^{-7} C·cm^{-2}. In these cases, N_a is kept at 5×10^{15} cm^{-3}, a value that is commonly available using commercial silicon wafers. For a low Q'_{eff} of 1×10^{-8} C·cm^{-2} in Case_5, the covered part behaves as an accumulation-type transistor, while the uncovered part is a depletion type. Holes become dominant as Q'_{eff}

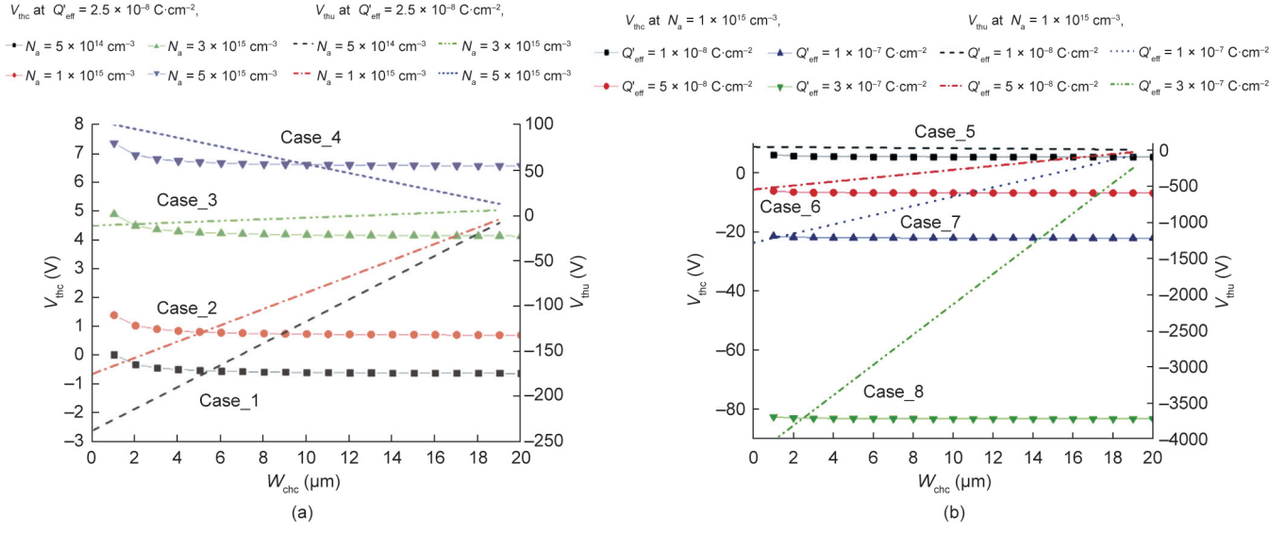

Fig. 3. Relationship between the threshold voltages V_{thc} and V_{thu}, and electrical parameters at different width positions. (a) Net concentration of ionized acceptors in the substrate N_a; (b) effective channel charge density Q'_{eff}. Symbol lines indicate the threshold voltage in the covered channel area V_{thc}, and dotted lines indicate the threshold voltage in the covered channel area V_{thu}. Case_1–Case_4: N_a increases from 5×10^{14} to 5×10^{15} cm^{-3}, while Q'_{eff} is kept low at 2.5×10^{-8} C·cm^{-2}; Case_5–Case_8: Q'_{eff} increases from 1×10^{-8} to 3×10^{-7} C·cm^{-2}, while N_a is kept at 1×10^{15} cm^{-3}.

increases above 5×10^{-8} C·cm^{-2}, allowing both areas to function as depletion-type transistors.

The relationship between the threshold voltage V_{th} and the geometry parameters L_{ch} and Z_{air} is shown in Fig. 4, where N_a and Q'_{eff} are set at 1×10^{14} cm^{-3} and 2.5×10^{-7} C·cm^{-2}, respectively. V_{thc} has a strong negative correlation with the air gap Z_{air} as the effective gate height Z'_{effc} increases. However, V_{thc} rarely changes for different channel lengths L_{ch}. V_{thu} increases slowly with an increase in channel length L_{ch}, but decreases significantly with an increase in the air gap Z_{air} for the same reason as V_{thc}. Therefore, the desired working types are achievable through appropriate assignment of electrical and geometry parameters. A nonzero gate voltage inducing a conducting channel in an accumulation-type device can probably produce an electrostatic force between the movable gate and substrate, resulting in undesirable vertical interference during operation [28]. The channel of a depletion-type device is conducted, although the potential difference is zero. Thus, electrostatic forces are eliminated. In other words, a depletion type is strongly expected for LMGFET devices. Therefore, the following design analysis is based on the norm that an LMGFET is free from electrostatic forces with a fixed gate voltage of 0 V.

2.3. Output channel current

The surface current density in two channel areas differs from each other. Thus, the current between the drain and source electrode in each area should be calculated individually, and the total output current should be their sum. By integrating the density of the channel surface carriers between two electrodes [29], the output current in the covered area I_{dsc} and the output current in the uncovered area I_{dsu} are defined as follows:

$$I_{dsc} = \frac{W_{chc}\mu'_{effc}Z'_{effc}}{L_{ch}\varepsilon_0}\left(V_{gs} - V_{thc} - \frac{1+F_{Bc}}{2}V_{ds}\right)V_{ds} \tag{8}$$

$$I_{dsu} = \frac{W_{chu}\mu'_{effu}Z'_{effu}}{L_{ch}\varepsilon_0}\left(V_{gs} - V_{thu} - \frac{1+F_{Bu}}{2}V_{ds}\right)V_{ds} \tag{9}$$

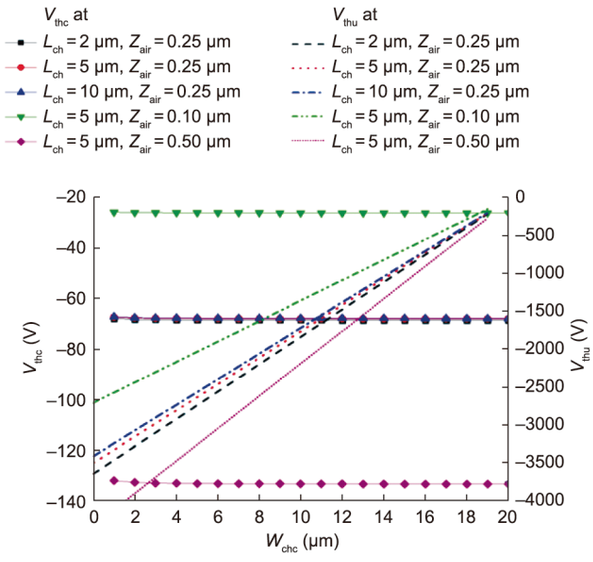

Fig. 4. Relationship between the threshold voltage V_{th} and the geometry parameters L_{ch} and Z_{air} at different width positions.

where $F_{Bc/u} = \frac{F_S\sqrt{2qN_a\varepsilon_{si}}}{4\sqrt{|\varphi_B - V_{bs}|}} + F_{Nc/u}$ is a voltage modulation coefficient in the covered and uncovered areas; μ'_{effc} and μ'_{effu} are the effective carrier mobilities in the covered and uncovered areas, respectively, which can be expressed as follows:

$$\mu'_{effc} = \frac{\mu_0}{1 + \frac{\delta}{Z'_{effc}}(V_{gs} - V_{thc}) + \frac{\mu_0}{V_{max}L_{ch}}V_{ds}} \tag{10}$$

$$\mu'_{effu} = \frac{\mu_0}{1 + \frac{\delta}{Z'_{effu}}(V_{gs} - V_{thu}) + \frac{\mu_0}{V_{max}L_{ch}}V_{ds}} \tag{11}$$

where μ_0 is the surface mobility of the carriers at a low electric field; δ is the vertical potential field factor; and V_{max} is the saturated velocity of the carriers. Effective carrier mobility is mainly regulated by the term $\frac{\delta}{Z'_{effu/c}}(V_{gs} - V_{thu/c})$, which accounts for the vertical potential degrading effect, and by the term $\frac{\mu_0}{V_{max}L_{ch}}V_{ds}$, which describes the velocity limitation and lateral potential degrading effect [30]. μ'_{effc} and μ'_{effu} change when the gate shifts to different channel widths and heights. I_{ds} approaches the value of the saturated current I_{dsat} when V_{ds} increases to a saturated status.

As discussed in our previous work [25], the saturated voltage of small-scale devices results from a saturated velocity. The saturated voltages in the covered area V_{dsatc} and in the uncovered channel area V_{dsatu} are expressed as follows:

$$V_{dsatc} = \frac{V_{gs} - V_{thc}}{1+F_{Bc}} + \frac{V_{max}L_{ch}}{\mu'_{effc}} - \sqrt{\left(\frac{V_{gs} - V_{thc}}{1+F_{Bc}}\right)^2 + \left(\frac{V_{max}L_{ch}}{\mu'_{effc}}\right)^2} \tag{12}$$

$$V_{dsatu} = \frac{V_{gs} - V_{thu}}{1+F_{B}} + \frac{V_{max}L_{ch}}{\mu'_{effu}} - \sqrt{\left(\frac{V_{gs} - V_{thu}}{1+F_{Bu}}\right)^2 + \left(\frac{V_{max}L_{ch}}{\mu'_{eff}}\right)^2} \tag{13}$$

where I_{dsat} is the maximum controllable output for LMGFET devices and is directly affected by the threshold voltage applied at the drain electrode. Fig. 5 illustrates the relationship between the threshold voltage in the two areas and the electrical parameters (with acceptor concentration N_a and effective channel charge density Q'_{eff}) and geometrical parameters (with air gap Z_{air} and channel length L_{ch}). Aside from the similar parameters in the last calculation, the voltage difference between the substrate and source electrode V_{gs} is 0 V, the carrier surface mobility μ_0 is 700 cm^2·V^{-1}·s^{-1} [31], and the saturated velocity V_{max} is 8×10^6 cm·s^{-1} [32]. The saturated voltages of the two areas decrease with an increase in N_a and Q'_{eff}; they also decrease with a decrease in the corresponding channel width (W_{chc}/W_{chu}). More specifically, the decreasing amplitude due to a small width becomes distinct with an increase in N_a and Q'_{eff}. The green lines in Fig. 5(a) correspond to Case_2 in Table 1. The covered channel area is currently broken off, so the saturated voltage in the covered area is 0. The geometric parameters exhibit an opposite influence to the electrical ones. V_{dsatc} increases with an increase in L_{ch} and Z_{air}, as shown in Fig. 5(b). V_{dsatu} increases with an increase in L_{ch} and is insensitive to the change in the air gap Z_{air}. For a channel width W_{chu} of 10 μm, V_{dsatu} only changes by 0.18 V when Z_{air} changes from 0.1 to 0.5 μm.

The adopted saturated voltage is set to the lowest value during the gate's lateral movement to analyze the saturated current. The current I_{ds} is assumed to be constant if the applied voltage exceeds the saturated value in each area. A large Q'_{eff} or lower N_a results in a large I_{dsat} in two areas due to the large absolute value of the threshold voltages V_{thc} and V_{thu}. The saturated current is approximately zero when only the uncovered channel works in this case, as shown by the green lines of Fig. 6(a). The deformation sensitivity

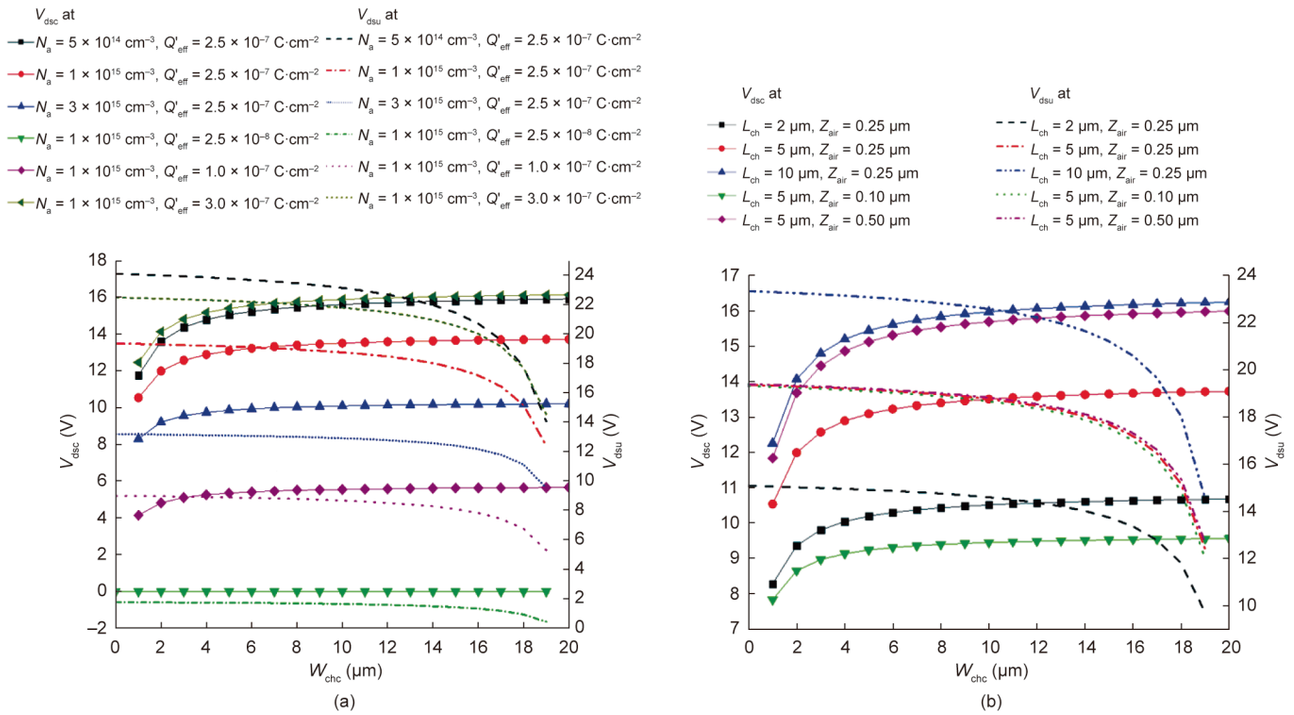

Fig. 5. Relationship between the saturated voltages V_{dsc} and V_{dsu}, and the electrical parameters and geometry parameters at different width positions. (a) Doped concentration of substrate N_a with effective channel charge density Q'_{eff}; (b) channel length L_{ch} and air gap Z_{air}. L_{ch} is 5 μm and Z_{air} is 0.25 μm for (a), while Q'_{eff} is 2.5 × 10^{-8} C·cm^{-2} and N_a is 1 × 10^{15} cm^{-3} for (b).

S is defined as the slope of the channel current curves and can be used to evaluate the electrical performance of the device when the gate moves laterally. The sensitivity S improves with an increase in the channel length L_{ch}. For an air gap Z_{air} of 0.25 μm, S increases from 13.144 to 17.140 μA·μm^{-1} when L_{ch} decreases from 10 to 2 μm. However, the device operation stability should be considered, because a small device size can result in a large potential field between the drain and source electrode and can easily break down the device. The air gap Z_{air} has a very large effect on the channel current I_{ds} and sensitivity S. For the device with a channel width W_{ch} of 10 μm and a channel length of 5 μm, the channel current I_{ds} increases from 1509.744 to 1796.400 μA when Z_{air} decreases from 0.5 to 0.1 μm. However, S decreases from 34.634 to 8.314 μA·μm^{-1} during this period, as shown in Fig. 6(b). This condition indicates that the output produced from undesirable vertical movement can be several times greater the current change from lateral movement. Therefore, a decoupling design is required to eliminate the interference from vertical movement, as discussed in the next section.

3. Sensor design and interconnection configuration

The proposed sensor utilizes an epoxy-type polymer photoresist, SU-8, as the structural material, which is an ideal material to fabricate LMGFET devices for the following reasons: First, SU-8 has a relatively low elastic modulus of 4–5 GPa, high mechanical strength, and stable chemical stability after ultraviolet (UV) exposure [33,34]. Second, SU-8 is a negative thick-film photoresist and can be used fabricate structures with a high aspect ratio [35]. These features make SU-8 suitable to serve as the structural material of laterally movable structures. Third, it is easy to uniformly deposit SU-8 on the substrate by utilizing a spin-coater or spray-coater, even for unleveled surfaces [36]. Finally, SU-8 can be easily patterned by UV exposure and developed in a propylene glycol methyl ether acetate solution, which is very much considerably more operable than etching materials, such as metal and silicon. In this research, an SU-8-based LMGFET force sensor with a movable sandwich structure is proposed, as discussed in the following section.

3.1. Movable structure design

The movable structure and the substrate are two main components in the device, as shown in Fig. 7(a). The movable structure contains a probe and a center mass supported by straight beams. Fig. 7(b) shows the sandwich gate structure in which a gold gate electrode layer is fully covered by two photoresistive SU-8 layers. Gold is a common metal material in most labs and has been demonstrated to have excellent adhesion to SU-8 [37]. The thickness of the lower SU-8 structural layer should be small in order to decrease the effective gate gap and effective capacitance. Two series of gold gate arrays, S1 and S2, are set in the center mass with an offset distance D_{off}. In each series, two gate arrays lie symmetrically about with respect to the lateral lines Line_1 and Line_2. The gates in two series have the same width W_g and length L_g. The corresponding drain, source electrodes, and gate insulator layer are positioned underneath the gate arrays. The channel region has width W_{ch} and length L_{ch} and lies between the drain and the source electrode. In the initial state, the gate covers half of the channel width, as shown in Fig. 7(c).

When a lateral force F_Y is applied at the probe, the beams are involved in bending deformation. The gate arrays in the center mass move laterally and change the width of the channel area, which is expressed as follows:

$$W_{F_Y} = \frac{F_Y L_b^3}{48 E I_Y} \tag{14}$$

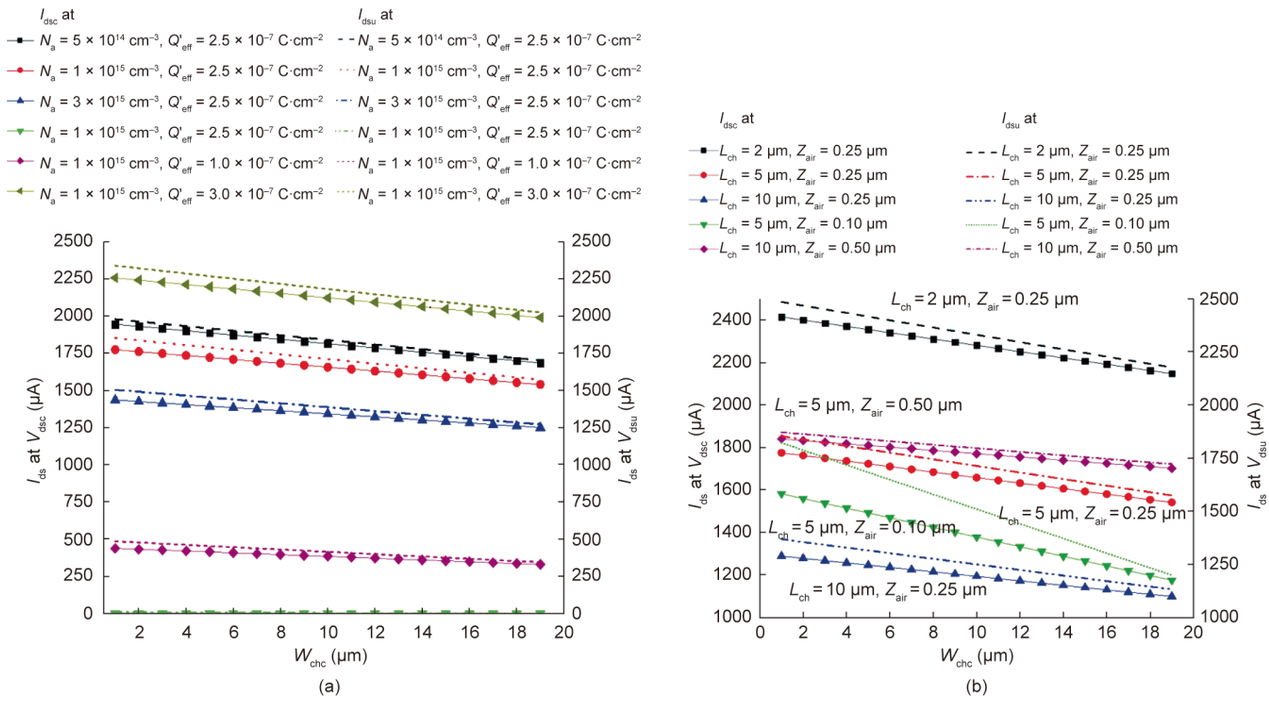

Fig. 6. Relationship between the saturated channel currents I_{dsc} and I_{dsu}, and the electrical parameters and geometry parameters at different width positions. (a) Net concentration of ionized acceptors in the substrate N_a with effective channel charge density Q'_{eff}; (b) channel length L_{ch} and air gap Z_{air}. L_{ch} is 5 μm and Z_{air} is 0.25 μm for (a), and Q'_{eff} is 2.5 × 10^{-8} C·cm^{-2} and N_a is 1 × 10^{15} cm^{-3} for (b).

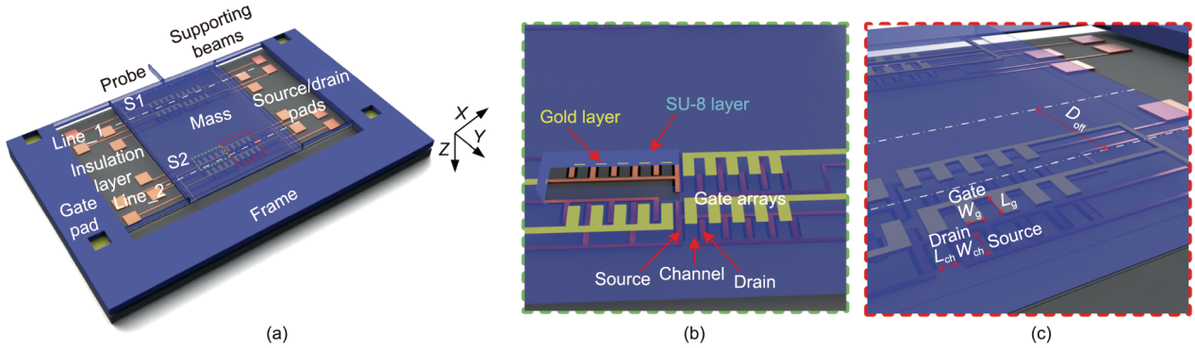

Fig. 7. Schematics of the proposed LMGFET force sensor. (a) Movable structure design; (b) movable sandwich structure containing a gold gate array layer and two photoresistive SU-8 layers; (c) arrangement and dimension of the movable gate arrays. The coordinate axis direction in all 3D models is based on the principle that the positive direction of the *Z*-axis is from the upper movable structure to the substrate, the positive direction of the *Y*-axis is from the sensor probe to the end of the movable structure, and the positive direction of the *X*-axis is from the left side to the right side of the sensor. S1, S2: two series of gold gate arrays; Line_1, Line_2: lateral lines; W_g: gate width; L_g: gate length; D_{off}: offset distance.

where W_{F_Y} is the structure deformation along *Y*-axis under F_Y; *E* is the Young's modulus of the structural materials; $I_Y = \frac{W_b T_b^3}{12}$ is the moment inertia of the beam vertical section; and L_b, W_b, and T_b are the length, width, and thickness of the supporting beam, respectively. When a vertical force F_Z is applied, the structure experiences a vertical force applied at mass center F'_Z and a force-induced moment $M_X = F_Z(L_p + \frac{1}{2}L_m)$ (where L_p is the probe length and L_m is the center mass length), which involve a vertical translation Z_F and a rotation around the *X*-axis for mass θ_X, as shown in Fig. 8; their expressions are

$$Z_F = \frac{F_Z L_b^3}{48 E I_Z} \tag{15}$$

$$\theta_X = \frac{M_X L_b^3}{24 E I_Z (L_m - L_b)} \tag{16}$$

where $I_Z = \frac{T_b W_b^3}{12}$ is the moment inertia of the beam horizontal section. On this basis, a line with a distance of D_{off} exists away from the mass center line and has zero vertical displacement. This line is expressed as follows:

$$D_{off} = \frac{L_m - L_b}{2L_p + L_m} \tag{17}$$

The vertical displacement of the gate series from force F_Z is expressed as follows:

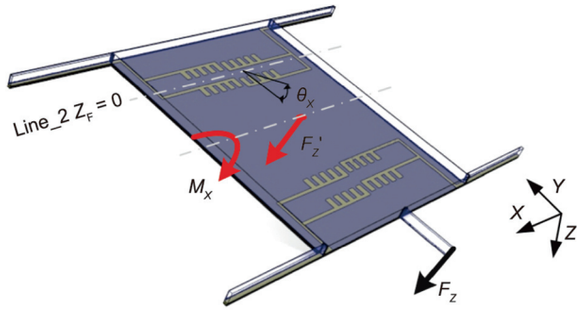

Fig. 8. Translation and rotation movements of a movable structure under vertical forces. Z_F, θ_X: vertical translation and rotation around the *X*-axis for mass, respectively.

$$Z_{F_Z} = \frac{F_Z L_b^3}{48EI_z} \pm D\frac{M_X L_b^3}{24EI_z(L_m - L_b)} \tag{18}$$

where ±*D* is the offset distance of the center lines between the gate array and mass, the minus sign before the *D* refers to the upper gate arrays in S2, and the plus sign refers to the downside gate arrays in S2. The deformation ratio between the lateral and vertical forces can be written as follows:

$$r = \frac{1}{\frac{T_b^2}{W_b^2}(1 \pm D\frac{2L_p + L_m}{L_m - L_b})} \tag{19}$$

A high *r* is achievable for structures whose thickness T_b is larger than the width W_b. Line_2 should be set at this D_{off} position, and the gate series S2 should be close to Line_2 in order to decrease undesired vertical movement. The straight beams cannot suppress or stretch. Thus, the structure rarely deforms along an *X*-axis force F_X. Therefore, the proposed movable structure will only be sensitive to force along the *Y*-axis and will be free from interference from other directions.

The proposed structure is simulated with ANSYS 15.0 to investigate its deformation behavior. The material and geometry parameters of the designed structure are given in Table 2. The geometry is modeled solely with an SU-8 structural layer, and the thin gold gate layer is ignored to reduce simulation complexity. In the simulations, the Young's modulus and Poisson's ratio of the SU-8 photoresist is 4.4 GPa [38] and 0.22 [39], respectively. The end of each beam is fixed, and a 1 nN force along the *Y*-/*Z*-axis is applied to the sidewall of the probe tip. Fig. 9 illustrates the deformation of gate series S2 under such forces. When a 1 nN lateral force is applied, the corresponding deformation is 1.961 nm, which is consistent with the theoretical value of 1.964 nm. Compared with the lateral movement under a *Y*-axis force, lateral movement caused by a *Z*-axis force is ignorable, as its value is approximately 0.00087 nm. The zero vertical deformation position D_{off} is approximately 673 μm away from the mass center. The vertical deformation of the gate series S1 is approximately 0.001 nm. The deformation ratio *r* is 1964, demonstrating the low cross-axis coupling effect in this structure.

Table 2
Material and geometry parameters of the designed structure.

Parameters	Value
Young's modulus of SU-8 photoresist	4.4 GPa
Poisson's ratio of SU-8 photoresist	0.22
Thickness of lower SU-8 structure layer	0.5 μm
Thickness of upper SU-8 structure layer	49.5 μm
Air gap Z_{air}	0.1 μm
Length of center mass L_m	2000 μm
Width of center mass W_m	1700 μm
Length of gate L_g	20 μm

3.2. Sensing configuration

Although the proposed structure rarely undergoes cross-axis deformation, undesired vertical deformation will inevitably bring interference to the channel current. Aside from the decoupling movable structure design, a sensing configuration is required to eliminate the cross-axis output coupling. A differential sensing configuration is normally adopted to compensate for loads from non-operation directions and for external disturbances, such as temperature and humidity. However, this method is unsuitable for LMGFET sensing because vertical movement of gate arrays different according to their position. In this research, a novel dual-differential sensing configuration is proposed, in which the underlying channel region is not aligned with the gate arrays but is distributed anti-symmetrically about the center of Line_1 and Line_2, as shown in Fig. 10. Each transistor series is separated into four arrays: $S1_{LU}$, $S1_{LD}$, $S1_{RU}$, and $S1_{RD}$ are for series S1, while $S2_{LU}$, $S2_{LD}$, $S2_{RU}$, and $S2_{RD}$ are for series S2. The interconnection configurations of S1 and S2 are illustrated in Figs. 11(a) and (b), respectively. S2 is for lateral force detection, and S1 is for vertical force detection. This paper focuses on lateral force detection. Thus, the following description is conducted with series S2. I_{dsL} is the sum of the current of two left transistor series $S2_{LU}$ and $S2_{LD}$, and I_{dsR} is the sum of the current of two right transistor series $S2_{RU}$, $S2_{RD}$. These expressions can be written as follows:

$$\begin{aligned} I_{dsL} = {} & I_{ds1}(W_{chc} + W_{F_Y}, Z_{air} + Z_{F_Z}) \\ & + I_{ds2}(W_{chc} + W_{F_Y}, Z_{air} - Z_{F_Z}) \end{aligned} \tag{20}$$

$$\begin{aligned} I_{dsR} = {} & I_{ds3}(W_{chc} + W_{F_Y}, Z_{air} + Z_{F_Z}) \\ & + I_{ds4}(W_{chc} + W_{F_Y}, Z_{air} - Z_{F_Z}) \end{aligned} \tag{21}$$

where I_{ds1}, I_{ds2}, I_{ds3}, and I_{ds4} are the current of the transistor series $S2_{LU}$, $S2_{LD}$, $S2_{RU}$, $S2_{RD}$, respectively.

Most vertical interferences are counteracted in Eqs. (20) and (21). The final sensor output can be measured with the potential difference between two circuit branches, $V_{out} = R \times (I_{dsL} - I_{dsR})$ (where *R* is the connected resistor in the readout circuit). The sensing performance of the proposed dual-differential configuration is illustrated in Fig. 12 and is compared with the normal differential method, where the channel region is aligned with the gate array. The difference between the initial output and that under the vertical displacement is measured with relative errors for the two methods, as shown in Figs. 12(a) and (b).

For a 1 nN force loaded in the sensor probe, the sandwich structure moves 1.961 nm laterally but 0.001 nm vertically. Therefore, the vertical displacement is set from 0.001 to 3.000 nm in order to investigate the sensing performance under vertical forces ranging from 1 nN to 3 μN. The relative errors of the two methods are negligible for a small vertical displacement of less than 0.03 nm. Because of the rapid increased C'_{effu}, the relative error of the differential channel current increases until W_{chc} reaches 7.5 μm. The relative error of the normal differential method at V_{dsc} reaches 4.53% for a 3 nm vertical displacement, and that of the proposed method is less than 0.01%. When W_{chc} reaches 10 μm, the relative errors solely resulting from the covered area exhibit a drop because C'_{effu} disappears. V_{dsu} has a higher change rate than V_{dsc} because C'_{effu} is more susceptible to air gap size than C'_{effc}; the relative errors at V_{dsu} show an increase compared with those at V_{dsc}, as shown in Fig. 12(b). The relative errors of the normal differential method at V_{dsu} increase to 2.24% and 4.76% for vertical displacements of 0.03 and 3.00 nm, respectively, but the largest relative error of the proposed configuration remains as low as 0.43%. Considering the

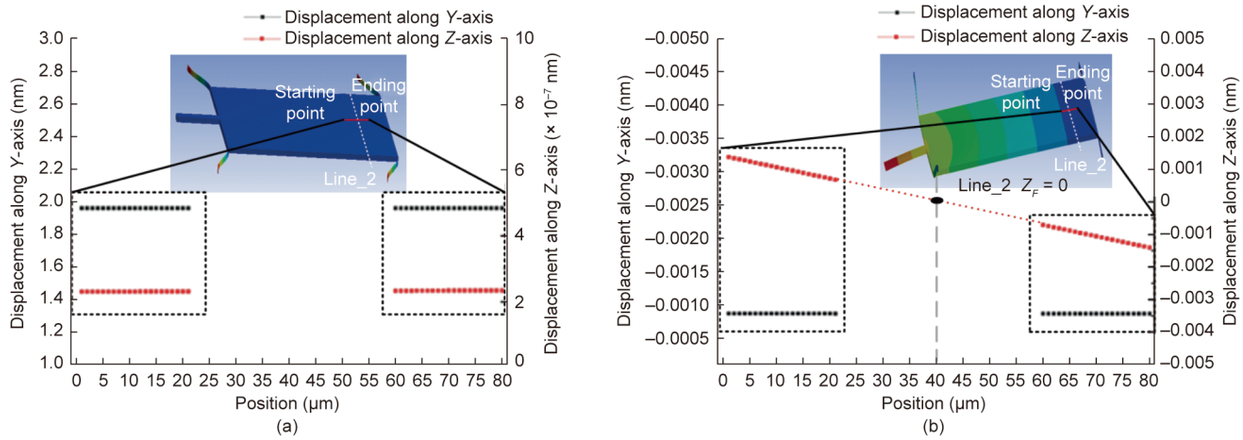

Fig. 9. Deformation of the movable structure under a 1 nN force. (a) Deformation of the gate series S1 under a force along the *Y*-axis; (b) deformation of the gate series S1 under a force along the *Z*-axis.

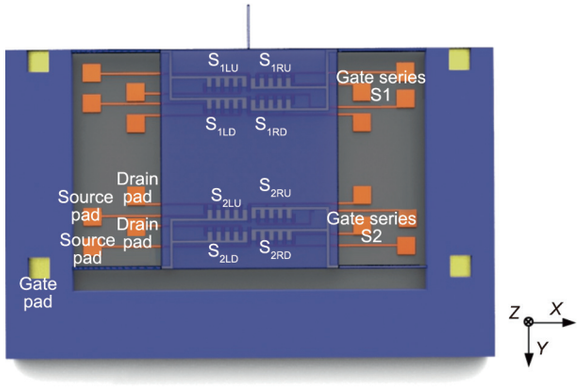

Fig. 10. The proposed dual-differential sensing configuration. $S1_{LU}$, $S1_{LD}$, $S1_{RU}$, and $S1_{RD}$ are transistor series for S1; $S2_{LU}$, $S2_{LD}$, $S2_{RU}$, and $S2_{RD}$ are transistor series for S2.

deformation behavior of the movable structure, a 3 nm vertical deformation of the gate series S1 demands a vertical force of 3 μN. The gate series cannot deform at 3 nm because the mass end face could touch the substrate under vertical forces below such a value. Therefore, the cross-axis coupling effect is thoroughly eliminated in the proposed dual-differential sensing configuration.

4. Model validation and sensor performance

4.1. Fabrication process

A simple but practicable fabrication is proposed for the presented LMGFET device, as shown in Fig. 13. A photoresist layer is deposited and patterned to define the drain and source electrode and its interconnections; the substrate is then ion-implanted to form phosphorus-doped areas. Through another patterned photoresistive layer, the channel area is defined and then doped with phosphorus ions but using different implantation doses and

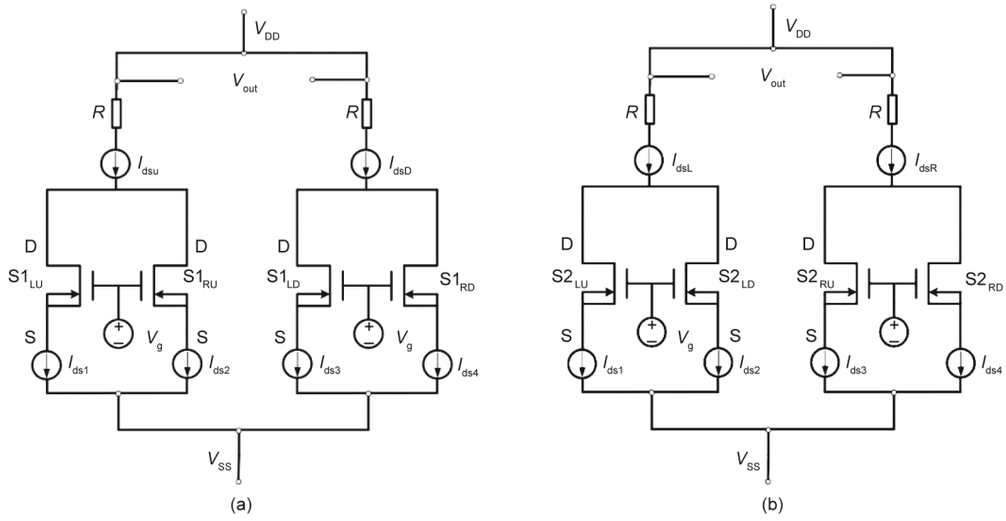

Fig. 11. Schematic of the proposed dual-differential configuration. (a) Interconnection of gate series S1; (b) interconnection of gate series S2. D: the common drain electrode; S: the common source electrode; V_{DD}: voltage applied at the common drain electrodes; V_{ss}: voltage applied at the common source electrode; V_g: voltage applied at the common gate electrodes. *R*: resistor; I_{dsU}: the sum of the current of two left transistor series $S2_{LU}$ and $S2_{RU}$; I_{dsD}: the sum of the current of two left transistor series $S2_{LD}$ and $S2_{RD}$; I_{dsL}: the sum of the current of two left transistor series $S2_{LU}$ and $S2_{LD}$; I_{dsR}: the sum of the current of two right transistor series $S2_{RU}$, $S2_{RD}$; I_{ds1}–I_{ds4}: the current of the transistor series $S2_{LU}$, $S2_{LD}$, $S2_{RU}$, $S2_{RD}$, respectively.

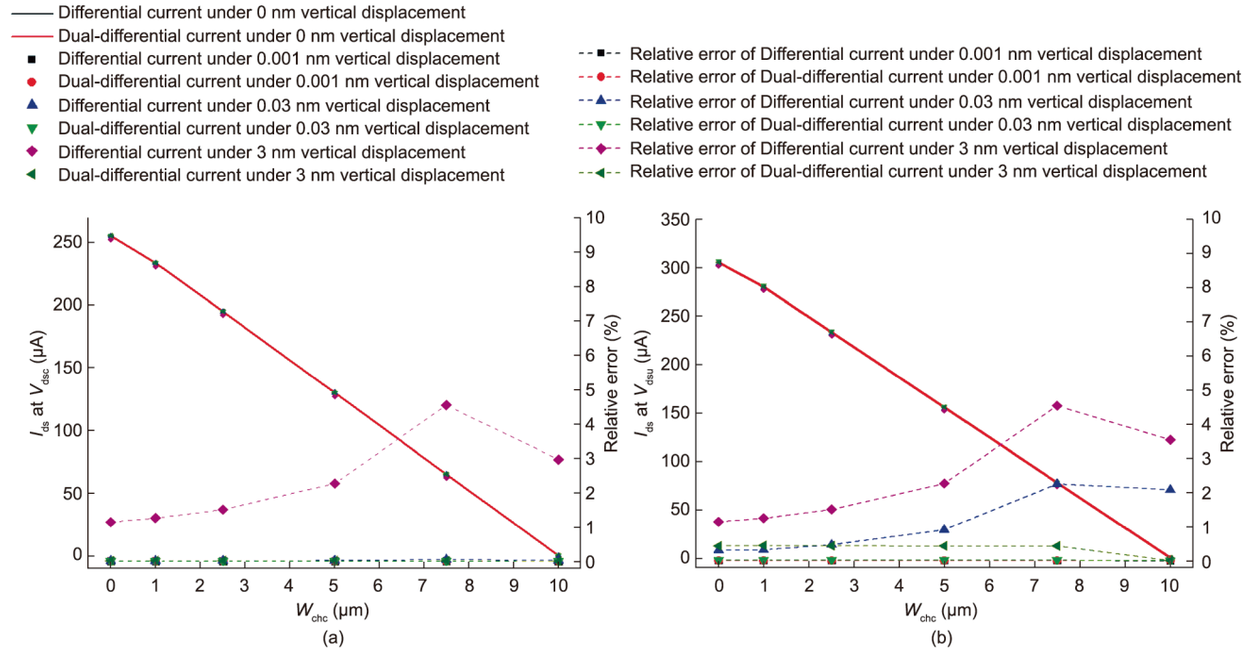

Fig. 12. Sensing performance of the proposed dual-differential configuration under different saturated voltages. (a) Channel current at saturated drain voltage V_{dsc}; (b) channel current at saturated drain voltage V_{dsu}. Straight lines indicate the output current under 0 nm vertical displacement, scatters indicate the output under different vertical displacements, and dashed lines with scatters represent the relative output error of the two sensing configurations.

energies. The implanted ions are activated through rapid thermal annealing. A gate insulation layer made of silicon nitride is deposited and then patterned to expose contact holes for source/drain interconnections. Subsequently, a sacrificial layer of silicon dioxide is deposited and patterned to expose the structure anchors and contact holes. A thin SU-8 structural layer is spun, exposed, and developed to act as the lower layer of the sandwich structure. A gold layer is then deposited and patterned to act as the gate arrays and pads of the drain and source electrodes. The substrate metal pad is formed through another gold layer deposited on the bottom side of the chip. Another thick SU-8 layer is spun to seal the gate array and is patterned for the upper sandwich structural layer. The substrate is patterned with deep reactive ion etching to expose the probe area. Finally, isotropic etching of the sacrificial silicon dioxide layer is conducted to release the movable sandwich structure.

The fabrication process is simulated using FEM Software Sentaurus 13.0; the adopted parameters are illustrated in Table 3 and the simulated LMGFET unit is shown in Fig. 14(a). The device is modeled as a single transistor to simplify the computation complexity, and the air gap and lower SU-8 structural layer are replaced with an effective silicon dioxide layer T'_{SiO_2} by using the following expression:

$$T'_{SiO_2} = \frac{\varepsilon_{SiO_2} Z_{air}}{\varepsilon_0} + \frac{\varepsilon_{SiO_2} T_{low\_SU-8}}{\varepsilon_{SU-8}} \tag{22}$$

Table 3
Parameters in fabrication simulation.

Parameters	Value
Acceptor concentration of silicon substrate N_a	1×10^{15} cm^{-3}
Thickness of insulator silicon nitride T_{insu}	100 nm
Thickness of gold gate T_g	0.2 μm
Thickness of effective silicon dioxide T_{insu}	1 μm
Length of channel L_{ch}	5 μm
Width of channel W_{ch}	20 μm
Implanted depth of source/drain X_j	0.5 μm
Implanted depth of channel	0.15–0.30 μm

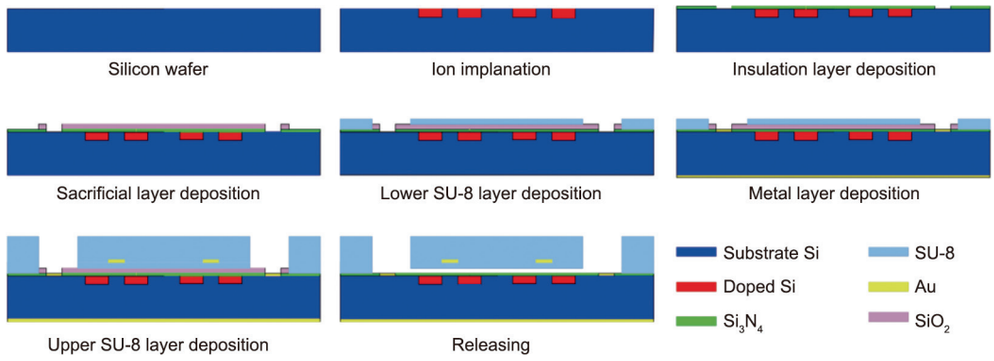

Fig. 13. Flow chart of the proposed fabrication process.

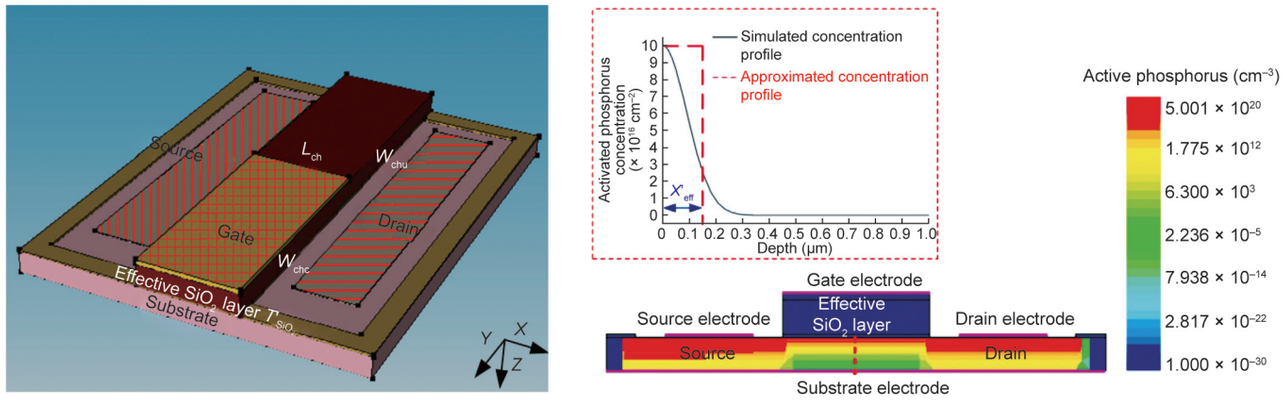

Fig. 14. Simulation of the proposed fabrication process. (a) 3D LMGFET unit in the simulation. (b) Implantation concentration in the simulated device; (upleft) extracted implantation ion profile along the dotted line in the channel area. X'_{eff}: the effective implantation depth.

where $T_{low\_SU\text{-}8}$ and $\varepsilon_{SU\text{-}8}$ are the thickness and permittivity of the lower SU-8 layer, and ε_{SiO_2} is the permittivity of silicon dioxide. The peak implanted ion concentration in the channel area is 1×10^{17} cm^{-2}, which is achievable in the bath fabrication process as discussed in our previous work [25]. The characteristic of how the distribution of channel impurities influences the channel current is investigated by setting different ion implantation depths from 0.150 to 0.300 μm. Fig. 14(b) shows a cross-section view of the activated implanted phosphorous distribution at an implantation depth of 0.275 μm. The inset shows the extracted concentration profile of active phosphorus in the channel region for the device in Fig. 14(a). A rectangular approximation is modeled to describe the concentration profile, as shown by the read dotted line in Fig. 14(b). The effective channel charge density Q'_{eff} is set as the product of the peak phosphorus density and the effective implantation depth. Table 4 lists the derived electrical parameters at different implantation depths.

4.2. Electrical model validation

Four different electrodes are set in the gate, source, drain, and substrate region and modeled as red grids to investigate the electrical output behaviors, as shown in Fig. 14(a). A voltage of 0 is applied to the gate, source, and substrate electrodes, because the fabricated transistor is a depletion-type device. Fig. 15(a) shows the channel output current I_{ds} characteristics under different chan-

Table 4
Extracted parameters under different implantation depths.

Implantation depth (μm)	X'_{eff} (μm)	Q'_{eff} ($C{\cdot}cm^{-2}$)	V_{dsatc} (V)	V_{dsatu} (V)
0.150	0.0791	1.266 × 10^{-7}	7.127	10.658
0.200	0.1073	1.717 × 10^{-7}	9.585	13.767
0.250	0.1367	2.187 × 10^{-7}	11.978	16.812
0.275	0.1509	2.414 × 10^{-7}	13.094	18.234
0.300	0.1661	2.658 × 10^{-7}	14.270	19.737

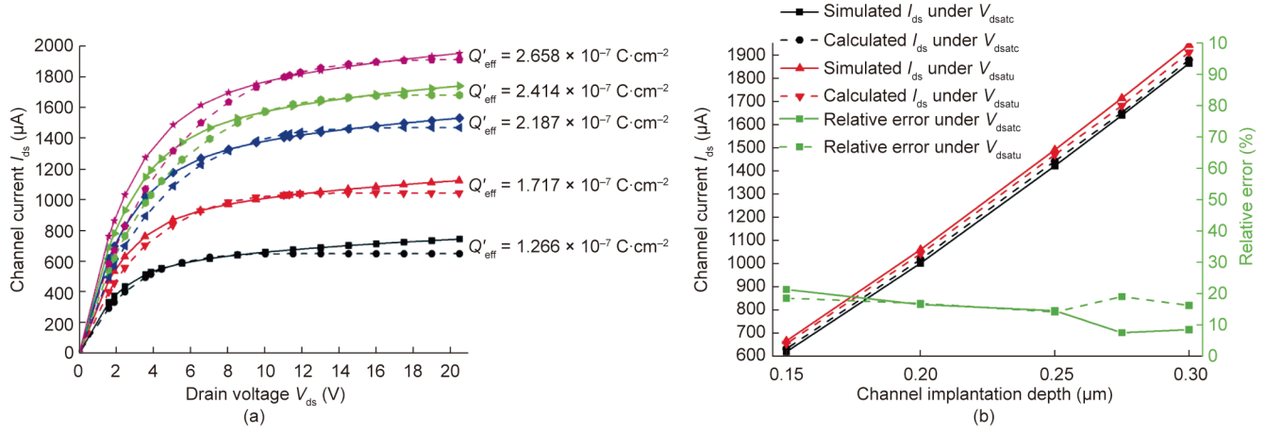

Fig. 15. Channel output current I_{ds} characteristics under different implantation depths. (a) Relationship between channel current I_{ds} and applied drain voltage V_{ds}; (b) saturated channel current I_{ds} and the corresponding relative errors between the calculated and simulated results. Solid lines indicate the simulated channel current, while dotted lines indicate the calculated channel current.

nel implantation profiles when the applied drain voltage V_{ds} increases from 0 to 20.5 V. When the implantation depth is 0.15 μm, the theoretical dotted line agrees well with the solid simulated line throughout the whole voltage range. The difference between the theoretical and simulated lines increases as the implantation depth increases. More specifically, the calculated current is smaller than that of the simulation for a low drain voltage, indicating that the proposed model is conservative in the non-saturation region. This characteristic is associated with the errors from the implantation approximation. However, the saturation region exhibiting the maximum controllable measuring sensitivity is the focus of this research, in which the theoretical calculation and simulations are in excellent accordance for all implantation depths. The calculated channel current is compared with the simulated one at the saturated voltages V_{dsc} and V_{dsu}; their relative errors are all less than 2% and are shown in Fig. 15(b).

The theoretical model is validated using the experimental data from Ref. [24] and is compared with the literature-adopted model, which assumes a constant effective gate capacitance in the uncovered channel area C'_{effu} and utilizes a regulation parameter for estimating the modulation effects. The experimental parameters extracted from Ref. [24] are listed in Table 5. In this study, the effective gate capacitance in the uncovered channel area C'_{effu} is constant and derived from the covered width W_{chc} of 18 μm. In fact, C'_{effu} should increase with the increase in W_{chc}, as discussed in Section 2. Fig. 16 provides a comparison of the calculated channel current from the proposed model and the model in Ref. [24]. The two models show similar accuracy for 18 μm W_{chc}. The proposed model presents a close estimation for the outputs under the covered channel widths W_{chc} of 0 and 60 μm. The largest relative error of the proposed model is 1.51% for a W_{chc} of 0 and 2.63% for a W_{chc} of 60 μm. However, those of the improved model are 6.64% and 5.84%, respectively. Therefore, the proposed model is more accurate than the previous model for LMGFET performance analysis.

4.3. Discussion of sensor performance

For sensor performance evaluation, the output channel current of the proposed sensor is obtained at different gate positions. Fig. 17 presents the saturated channel currents I_{dsatc} and I_{dsatu} of the simulations and calculation for an implantation depth of 0.275 μm. The saturated voltages V_{dsatc} and V_{dsatu} are set to 10.2 and 12.1 V, respectively, which are the lowest values during sensor operation. The relative error between the theoretical and simulated saturated currents is 3.88% and 5.64% at 0 μm W_{chc}. The mismatch under the condition of a small covered channel width mainly results from the estimation error of the capacitance expression (Eq. (2)). The relative error becomes less than 3.80% for W_{chc} > 1 μm. The sensitivity of the proposed device is 8.39 and 9.12 μA·nN^{-1} for the saturated voltages V_{dsatc} and V_{dsatu}, respectively. Due to the low stiffness of the SU-8 movable structure, the force sensitivity of the proposed LMGFET sensor is 4.65 μA·nN^{-1}, which is lower than that of our previous VMGFET device, which had a value of 12.53 μA·nN^{-1} [25]. Nevertheless, it is much higher than those of previous VMGFET devices with values of 3.24 [22] and 0.05 μA·nN^{-1} [23], and higher than that of a reported LMGFET device with a value of 0.01 μA·nN^{-1} [24]. The nonlinearity experiences a slight fluctuation because the transistor in either the covered channel area or the uncovered area disappears when the

Table 5
Experimental parameters of the fabricated LMGFET device [24].

Parameters	Value
Length of channel L_{ch}	30 μm
Total channel width $W_{ch} = W_{chc} + W_{chu}$	60 μm
Studied covered channel width W_{chc}	0, 18, 60 μm
Gate oxide thickness T_{insu}	27 nm
Acceptors concentration of silicon substrate N_a	1×10^{15} cm^{-3}
Effective channel charge density Q'_{eff}	2.37×10^{-7} C·cm^{-2}
Work function difference φ_{MS}	−0.30 V
Effective gate oxide capacitance in covered area C'_{effc}	1.55×10^{-8} F·cm^{-2}

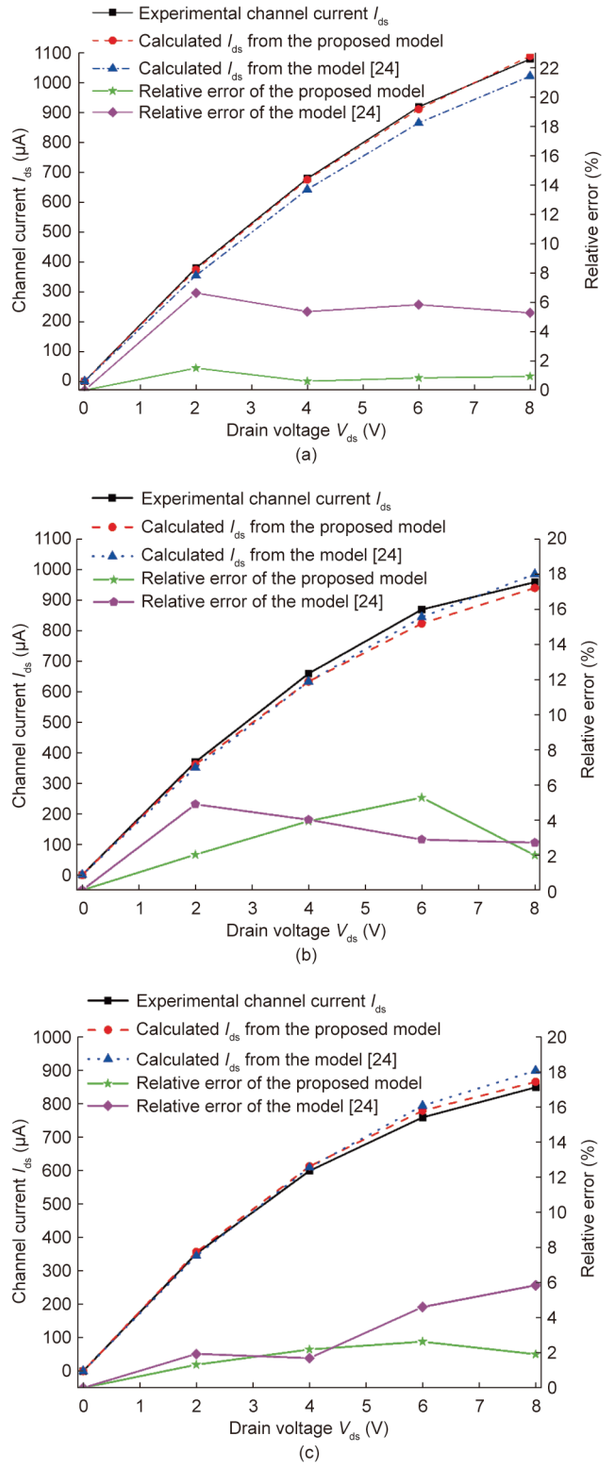

Fig. 16. Theoretical calculation and experimental measurement of channel current I_{ds}. (a) Gate fully uncovers the channel area, W_{chc} = 0 μm; (b) gate partially covers the channel area, W_{chc} = 18 μm; (c) gate fully covers the channel area, W_{chc} = 60 μm.

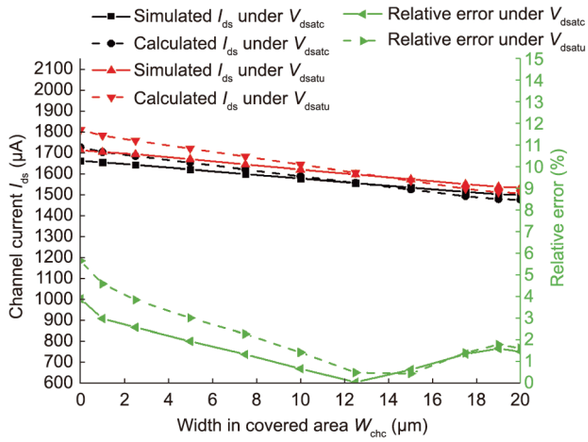

Fig. 17. Theoretical calculation and experimental measurement of channel current I_{ds} under different channel widths W_{chc}.

channel is fully covered or exposed. The nonlinearity approaches 0.19% and 0.78% for a W_{chc} ranging from 2.5 to 17.5 μm and from 1 to 19 μm, respectively, which is much less than that of existing MGFET devices. The measurement range of the proposed sensor is ±5.10 μN, which is relatively less than that of the LMGFET device in Ref. [24] but much larger than those of VMGFET devices [22,23,25].

To evaluate the overall sensing performance, the product of the sensitivity, linearity, and measurement range is calculated as a merit factor, as shown in Table 6 [22–25]. The proposed sensor exhibits the largest merit factor of 47.07 mA among existing MGFET devices, indicating that a delicate tradeoff has been made between high sensing accuracy and a large measurement range for the proposed sensor. All these characteristics make the proposed sensor a suitable choice for the measurement of ultralow forces below the nano-newton level, especially for biomedical applications requiring a large measurement range, such as cell deformation squeezing and cellular membrane penetration.

5. Conclusions

In this paper, an LMGFET micro force sensor was proposed and comprehensively analyzed. The electrical behavior of the small LMGFET unit was theoretically modeled into two individual parts and tested with simulations and experimental data. The proposed sensor exhibited improved accuracy and capability for device performance evaluation before mass fabrication. A novel sandwich structure containing a gold gate array layer and two covered SU-8 photoresist layers was developed by decoupling multiple gate arrays and using a dual-differential sensing configuration. The output current under cross-axis loadings was considerably suppressed. The electrical and structural parameters of LMGFET devices were fully analyzed in order to optimize the sensor performance, and a practicable fabrication process was developed and simulated. The proposed sensor exhibits considerably high sensitivity, linearity, and a large measurement range, making it a versatile sensing tool for biomedical micromanipulation tasks.

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Compliance with ethics guidelines

Wendi Gao, Zhixia Qiao, Xiangguang Han, Xiaozhang Wang, Adnan Shakoor, Cunlang Liu, Dejiang Lu, Ping Yang, Libo Zhao, Yonglu Wang, Jiuhong Wang, Zhuangde Jiang, and Dong Sun declare that they have no conflict of interest or financial conflicts to disclose.

References

[1] Dostanic M, Windt LM, Stein JM, van Meer BJ, Bellin M, Orlova V, et al. A miniaturized EHT platform for accurate measurements of tissue contractile properties. J Microelectromech Syst 2020;29(5):881–7.
[2] Nakahara K, Sakuma S, Kawahara M, Takahashi M, Arai F. Time-lapse mechanical characterization of zona pellucida using a cell carrier chip. J Microelectromech Syst 2018;27(3):464–71.
[3] Corbin EA, Adeniba OO, Ewoldt RH, Bashir R. Dynamic mechanical measurement of the viscoelasticity of single adherent cells. Appl Phys Lett 2016;108(9):093701.
[4] Pu H, Chen H, Sun Yu, Liu Na, Yu J, Yang Y, et al. Micropipette aspiration of single cells for both mechanical and electrical characterization. IEEE Trans Biomed Eng 2019;66(11):3185–91.
[5] Tsukagoshi T, Nguyen TV, Shoji KH, Takahashi H, Matsumoto K, Shimoyama I. Cellular dynamics of bovine aortic smooth muscle cells measured using MEMS force sensors. J Phys D Appl Phys 2018;51(14):145401.
[6] Pan P, Qu J, Zhang W, Dong X, Wei W, Ru C, et al. Robotic stimulation of freely moving *Drosophila* larvae using a 3D-printed micro force sensor. IEEE Sens J 2019;19(8):3165–73.
[7] Zhang W, Pan P, Wang X, Chen Y, Rao Y, Liu X. Force-controlled mechanical stimulation and single-neuron fluorescence imaging of *Drosophila* larvae. IEEE Robot Autom Lett 2021;6(2):3736–43.
[8] Wei Y, Xu Q. Design and testing of a new force-sensing cell microinjector based on small-stiffness compliant mechanism. IEEE/ASME Trans Mechatron 2021;26(2):818–29.
[9] Wei Y, Xu Q. A survey of force-assisted robotic cell microinjection technologies. IEEE Trans Autom Sci Eng 2019;16(2):931–45.
[10] Cailliez J, Boudaoud M, Mohand-Ousaid A, Weill–Duflos A, Haliyo S, Régnier S. Modeling and experimental characterization of an active MEMS based force sensor. J Micro-Bio Robot 2019;15(1):53–64.
[11] Qu J, Zhang W, Jung A, Silva-Da Cruz S, Liu X. Microscale compression and shear testing of soft materials using an MEMS microgripper with two-axis actuators and force sensors. IEEE Trans Autom Sci Eng 2017;14(2):834–43.
[12] Grech D, Tarazona A, De Leon MT, Kiang KS, Zekonyte J, Wood RJK, et al. A quasi-concertina force-displacement MEMS probe for measuring biomechanical properties. Sens Actuators A Phys 2018;275:67–74.

Table 6
Performance comparison with existing MGFET devices.

	Sensitivity (μA·nN^{-1})[a]	Nonlinearity (%)	Deformation range (μm)	Measurement range (μN)	Merit factor (mA)
This work	4.65	0.78	±10.0	±5.10	47.07
LMGFET [24]	0.01	7.28	±30.0	±14.50	0.32
VMGFET [25]	12.53	1.35	0.3	0.42	5.24
VMGFET [22]	3.24	11.12	0.2	0.12	0.35
VMGFET [23]	0.05	17.75	1.0	Na	Na

Na: not available.
[a] Sensitivity is unified into the same unit.

[13] Stavrov VT, Shulev AA, Hardalov CM, Todorov VM, Roussev IR. All-silicon microforce sensor for bio applications. In: Proceedings of SPIE Microtechnologies; 2013 Apr 24–26; Grenoble, France. SPIE; 2013. p. 87630Y.
[14] Xie Y, Sun D, Liu C, Tse HY, Cheng SH. A force control approach to a robot-assisted cell microinjection system. Int J Robot Res 2010;29(9):1222–32.
[15] Xie Y, Zhou Y, Lin Y, Wang L, Xi W. Development of a microforce sensor and its array platform for robotic cell microinjection force measurement. Sensors 2016;16(4):483.
[16] Gao W, Zhao L, Jiang Z, Xia Y, Guo X, Zhao Z, et al. A novel MEMS force sensor based on laterally movable gate array field effect transistor (LMGAFET). In: Proceedings of 2017 IEEE 12th International Conference on Nano/Micro Engineered and Molecular Systems (NEMS); 2017 Apr 9–12; Los Angeles, CA, USA. IEEE; 2017. p. 723–7.
[17] Zang Y, Zhang F, Huang D, Gao X, Di C, Zhu D. Flexible suspended gate organic thin-film transistors for ultra-sensitive pressure detection. Nat Commun 2015;6:6269.
[18] Ajmera PK, Song IH. Laterally movable gate FET (LMGFET) for on-chip integration of MEMS with electronics. In: Proceedings of SPIE's 8th Annual International Symposium on Smart Structures and Materials; 2001 Mar 4–8; Newport Beach, CA, USA. SPIE; 2001. p. 30–7.
[19] Gao W, Shakoor A, Xie M, Chen S, Guan Z, Zhao L, et al. Precise automated intracellular delivery using a robotic cell microscope system with three-dimensional image reconstruction information. IEEE/ASME Trans Mechatron 2020;25(6):2870–81.
[20] Gao W, Shakoor A, Zhao L, Jiang Z, Sun D. 3D image reconstruction of biological organelles with a robot-aided microscopy system for intracellular surgery. IEEE Robot Autom Lett 2019;4(2):231–8.
[21] Kang HS, Lee KH, Yang DY, You BH, Song IH. Micro-accelerometer based on vertically movable gate field effect transistor. Nano-Micro Lett 2015;7(3):282–90.
[22] Aoyagi S, Suzuki M, Kogure J, Kong T, Taguchi R, Takahashi T, et al. Accelerometer using MOSFET with movable gate electrode: electroplating thick nickel proof mass on flexible Parylene beam for enhancing sensitivity. In: Proceedings of 2011 16th International Solid-State Sensors, Actuators and Microsystems Conference; 2011 Jun 5–9; Beijing, China. IEEE; 2011. p. 2030–3.
[23] Coe DJ, English JM, Lindquist RG, Kaiser TJ. Model of a MEMS sensor using a common gate MOSFET differential amplifier. J Phys D Appl Phys 2006;39(20):4353–8.
[24] Song IH, Ajmera PK. A laterally movable gate field effect transistor. J Microelectromech Syst 2009;18(1):208–16.
[25] Gao W, Jia C, Jiang Z, Zhou X, Zhao L, Sun D. The design and analysis of a novel micro force sensor based on depletion type movable gate field effect transistor. J Microelectromech Syst 2019;28(2):298–310.
[26] Zhang A, Zhang L, Tang Z, Cheng X, Wang Y, Chen KJ, et al. Analytical modeling of capacitances for GaN HEMTs, including parasitic components. IEEE Trans Electron Dev 2014;61(3):755–61.
[27] Bansal A, Paul BC, Roy K. An analytical fringe capacitance model for interconnects using conformal mapping. IEEE Trans Comput Des Integr Circuits Syst 2006;25(12):2765–74.
[28] Bao M, Yang H, Yin H, Shen S. Effects of electrostatic forces generated by the driving signal on capacitive sensing devices. Sens Actuators A Phys 2000;84(3):213–9.
[29] El-Mansy YA. Analysis and characterization of the depletion-mode IGFET. IEEE J Solid-State Circuits 1980;15(3):331–40.
[30] Sun SC, Plummer JD. Electron mobility in inversion and accumulation layers on thermally oxidized silicon surfaces. IEEE J Solid-State Circuits 1980;15(4):562–73.
[31] Arora N. MOSFET models for VLSI circuit simulation. Vienna: Springer Vienna; 1993.
[32] Coen RW, Muller RS. Velocity of surface carriers in inversion layers on silicon. Solid-State Electron 1980;23(1):35–40.
[33] Ge C, Cretu E. A sacrificial-layer-free fabrication technology for MEMS transducer on flexible substrate. Sens Actuators A Phys 2019;286:202–10.
[34] Nagai M, Tanizaki K, Shibata T. Batch assembly of SU-8 movable components in channel under mild conditions for dynamic microsystems: application to biohybrid systems. J Microelectromech Syst 2019;28(3):419–28.
[35] Ge C, Cretu E. Design and fabrication of SU-8 CMUT arrays through grayscale lithography. Sens Actuators A Phys 2018;280:368–75.
[36] Vinje J, Beckwith KS, Sikorski P. Electron beam lithography fabrication of SU-8 polymer structures for cell studies. J Microelectromech Syst 2020;29(2):160–9.
[37] Dai W, Lian K, Wang W. A quantitative study on the adhesion property of cured SU-8 on various metallic surfaces. Microsyst Technol 2005;11(7):526–34.
[38] Dai W, Lian K, Wang W. Design and fabrication of a SU-8 based electrostatic microactuator. Microsyst Technol 2007;13(3–4):271–7.
[39] Microchem. Datasheet of SU-8 2025–2075 [Internet]. Newton: Microchem; 2009 Sep 22 [cited 2021 Sep 3]. Available from: https://kayakuam.com/products/su-8-2000/.