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News & Highlights

Simplified Instruction Set Architecture Accelerates Chip Development and Wins the 2022 Draper Prize

Chris Palmer

Senior Technology Writer

The previously slow and steady rise in the adoption of a streamlined computer chip instruction set architecture (ISA), the fifth generation of reduced instruction set computer (RISC-V), has officially entered overdrive. In early February 2022, the silicon heavyweight Intel (Santa Clara, CA, USA) announced a big investment in the RISC-V ecosystem, part of a 1 billion USD fund launched by Intel to support partnerships between it and other companies developing new chip-based technology [1,2]. The move bolsters Intel's plans to grow its foundry business and is complemented by the company's simultaneously announced new membership in RISC-V International, the Zurich, Switzerland-based organization that governs the codification of the core and new extensions for RISC-V, a freely available, open-standard ISA first introduced in 2010 [1,2].

"Intel partnering with several RISC-V members is a huge signal to the industry about the growing interest and adoption of RISC-V," said Calista Redmond, chief executive officer of RISC-V International. "Intel recognizes that RISC-V will be a critical component for the success of its foundry endeavors, so the company is investing heavily in making it easier for companies to design RISC-V solutions."

The RISC-V market, though still relatively small, is expected to grow rapidly. The consulting and analytics firm Deloitte Global (New York City, NY, USA) predicts the market for RISC-V processing cores will double in 2022 compared to 2021 and double again in 2023 [3]. RISC-V revenue will increase more slowly, though, nearing 800 million USD in 2023, up from less than 400 million USD in 2021, and approaching 1 billion USD by 2024 [3].

At a basic level, the ISA in chips allows software to directly control hardware, and the chips that now drive most of the world's devices use two well-established—and proprietary—ISAs. Over the past several decades, Intel's x86 has maintained its position as the dominant ISA used in the chips in laptops, desktops, and server hardware. In contrast, most smartphones use ARM-based chips, primarily because they consume little power. But now a growing contingent of companies in the United States, Europe, and especially Asia sees RISC-V as an attractive alternative—and supplement—to these entrenched standards.

RISC-V is one of many RISC-based ISAs, including ARM, created over the years, for which four individuals were awarded the 2022 Charles Stark Draper Prize in March [4]. The moniker "reduced instruction set computer" reflects the aim of the prize recipients—Stephen B. Furber, professor of computer engineering at the University of Manchester, UK; John L. Hennessy, professor of computer science and electrical engineering at Stanford University in Palo Alto, CA, USA; David A. Patterson, professor emeritus at the University of California, Berkeley, CA, USA; and Sophie M. Wilson, a Cambridge University, UK-trained computer scientist—and their many collaborators to build smaller, lower-power but better-performing processors by decreasing the complexity of the core set of executable instructions [4]. With RISC-V, the result is a core of 47 instructions—paltry compared to x86's 1000-some instructions and ARM's roughly 500 [2,5]. And RISC-V is an extensible ISA, meaning that companies can implement the instruction set core and later expand it by adding defined extensions or creating their own to build bespoke processors.

This makes RISC-V-based chip designs easy to modify, allowing for greater flexibility when applied to the broad range of digital applications, from high-performance computing (HPC), self-driving vehicles and the Internet of Things (IoT) to storage, graphics, and artificial intelligence (AI) and machine learning [3]. "RISC-V is fairly sophisticated. It does not have 30 years of baggage, which makes it a 'clean-slate' architecture," said Balaji Baktha, chief executive officer and founder of RISC-V processor developer—and one of several new Intel partners—Ventana Micro Systems in Cupertino, CA, USA.

In addition to offering flexibility, being open standard also makes RISC-V an attractive option, particularly for startups wanting to design custom chips without spending the millions of dollars in license fees required to use proprietary chip architectures. Both factors have been cited as making RISC-V an increasingly popular chip architecture for companies such as the computing storage giants Seagate (Cupertino, CA, USA) and Western Digital (San Jose, CA, USA), as well as e-commerce giant Alibaba (Hangzhou, China) [6].

Being open standard also makes RISC-V appealing to companies that have lost or fear losing access to x86 or ARM, potentially due to export restrictions [7]. Choosing RISC-V eliminates that issue. Chinese companies make up more than a third of the membership of RISC-V International, including, among others, Huawei (Shenzhen, China) and Alibaba Cloud, with multiple large Chinese companies having announced their intention to use RISC-V chips [6]. In addition, China launched a research institute in late 2021

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devoted to RISC-V processor projects [8], Alibaba announced efforts to port Android to RISC-V [9], and a pair of Chinese firms—DeepComputing and Xcalibyte—have begun manufacturing the world's first RISC-V-based laptop in Shenzhen, China [10].

By climbing aboard the RISC-V bandwagon, Intel aims to help RISC-V development-focused companies, including announced partners Andes Technology (Hsinchu, China), Esperanto Technologies (Mountain View, CA, USA), SiFive (San Mateo, CA, USA), and Baktha's Ventana Micro Systems, more quickly innovate by prioritizing their manufacturing runs and working with them to co-develop manufacturing technology that optimizes their designs [1,2].

A primary goal of Intel's 1 billion USD fund is to implement a cost-effective modular design that integrates several types of processor cores within an individual chip package [1,2]. This will help the chip giant's new venture, Intel Foundry Services, manufacture chips that each contain multiple chiplet dies, with custom mixes of x86, ARM, and RISC-V cores. "People ask if Intel sees RISC-V as a threat," Baktha said. "Their investment shows otherwise. Allowing RISC-V to sit alongside x86 infrastructure makes things like data center innovation happen at a level never before possible."

Much of the interest in RISC-V is coming from demand for AI applications. For edge-based AI implementations where AI processes run and generate data on local devices like laptops, rather than in the cloud, "computing and AI need to come together in a unified architecture," said Baktha. "RISC-V is the only way to do it." Semiconductor consulting firm Semico Research (Phoenix, AZ, USA) estimates that RISC-V-based AI systems-on-a-chip (SoC)—integrated circuits consisting of all or most components of a computer—will see an average of 74% growth per year between now and 2027 [11]. Semico additionally projects RISC-V AI SoC for consumer IoT solutions to grow 140% per year over the same timeframe, along with 98% yearly growth for HPC markets like data center servers [11].

When initially released in 2010, RISC-V lacked the vector instructions required for the math of machine learning, including matrix multiplication. To overcome this gap, Esperanto engineers developed their own instructions, which they have incorporated into their new chip, the ET-SoC-1 (Fig. 1), marketed by the company as the first high-performance RISC-V AI chip [2]. The company specifically designed the ET-SoC-1 for power-efficient inference processing and to compete against powerful graphics processing unit (GPU) in AI-recommendation systems (which offer relevant suggestions to users based on data such as their demographics or prior behavior), primarily for e-commerce and social media firms [12]. At half the size of its primary competition, Nvidia's A100 chip, the ET-SoC-1 draws just one tenth the power of the A100 [2]. Several companies, including Samsung, are now exploring the use of the ET-SoC-1 in their devices [13].

Other companies with recently developed AI processors are using combinations of RISC-V and custom machine-learning acceleration technology. For example, the Hierarchical Learning Processor announced in January 2022 by San Jose, USA-based Ceremorphic combines RISC-V and ARM cores along with its own custom machine-learning and floating-point arithmetic units [14]. And Intel's forthcoming Mobileye EyeQ Ultra will have 12 RISC-V cores supplemented by proprietary neural-network accelerators, along with an ARM CPU, in a chip meant to supply intelligence for near fully autonomous driving [15]. Also turning to RISC-V to support autonomous driving is embedded AI processor firm Kneron (San Diego, CA, USA). Last November, the company began mass-producing its first RISC-V KL530 chip based on a new type of neural network that performs image classification tasks [16].

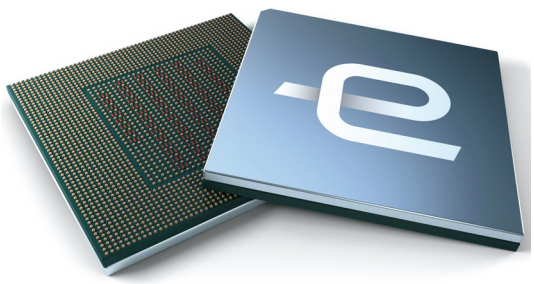

Fig. 1. Esperanto Technologies' ET-SoC-1 chip packs more than 1000 RISC-V cores onto a 570 mm^2 piece of silicon that consumes just 20 W in operation. Credit: Esperanto Technologies (public domain).

In June 2022, Intel, which already offers RISC-V-based Nios V processors, announced a collaboration with the Barcelona Supercomputing Centre in Spain to build a 400 million USD facility devoted to developing RISC-V processors for HPC, as well as specialized chips for AI and autonomous vehicles. A primary goal of the collaboration is to create zettascale systems 1000-times more powerful than today's fastest supercomputers, a milestone that Intel says it aims to achieve within the next five years [17,18].

While the future of RISC-V appears bright, several challenges remain for developers before the market can fully embrace the ISA [3]. Certain kinds of new RISC-V-based software compilers, processors, and computer designs must be built *de novo*, a time-consuming and expensive prospect. Also, while RISC-V is supported by several distributions of Linux, including Ubuntu, Debian, FreeBSD, NetBSD, and OpenBSD, it has yet to be adapted for some other widely used operating systems.

Regardless, like many of its promotors, Redmond focuses on the flexibility she sees RISC-V bringing to the world of computing. "For decades, custom silicon was only attainable for companies with huge design teams and budgets," Redmond said. "RISC-V enables design freedom across every domain and industry, making it possible for companies of all sizes to push the bounds of innovation and have an opportunity to compete."

References

[1] Intel launches $1 billion fund to build a foundry innovation ecosystem [Internet]. Santa Clara: Intel; 2022 Feb 7 [cited 2022 Jul 13]. Available from: https://www.intc.com/news-events/press-releases/detail/1525/intel-launches-1-billion-fund-to-build-a-foundry.

[2] Moore SK. RISC-V AI chips will be everywhere [Internet]. New York City: IEEE Spectrum; 2022 Feb 24 [cited 2022 Jul 5]. Available from: https://spectrum.ieee.org/risc-v-ai.

[3] Stewart D, Bucaille A, Kodama E, Crossan G. RISC-y business: could open chip standard RISC-V gain traction against dominant incumbents? [Internet]. New York City: Deloitte; 2021 Dec 1 [cited 2022 Jul 5]. Available from: https://www2.deloitte.com/us/en/insights/industry/technology/technology-media-and-telecom-predictions/2022/risc-v-open-source-cpu.html.

[4] 2022 Draper Prize recipients honored for contributions to the invention of RISC chips [Internet]. Washington, DC: National Academy of Engineering; 2022 Mar [cited 2022 Jul 23]. Available from: https://www.nae.edu/276632/2022-Draper-Prize-Recipients-Honored-for-Contributions-to-the-Invention-of-RISC-Chips.

[5] Bailey B. A minimal RISC-V [Internet]. San Jose: Semiconductor Engineering; 2022 Jan 13 [cited 2022 Jul 13]. Available from: https://semiengineering.com/a-minimal-risc-v/.

[6] Hsu J. RISC-V star rises among chip developers worldwide [Internet]. New York City: IEEE Spectrum; 2021 Apr 7 [cited 2022 Jul 5]. Available from: https://spectrum.ieee.org/riscv-rises-among-chip-developers-worldwide.

[7] Haranas M. Huawei selling x86 server business due to US sanctions: report [Internet]. Westborough: CRN; 2021 Nov 4 [cited 2022 Jul 13]. Available from: https://www.crn.com/news/data-center/huawei-selling-x86-server-business-due-to-u-s-sanctions-report.

[8] China opens new research institute to develop RISC-V processor project [Internet]. Beijing: TechNode; 2022 Apr 11 [cited 2022 Jul 5]. Available from: https://technode.com/2022/04/11/china-opens-new-research-institute-to-develop-risc-v-processor-project/.

[9] Mitchell R. Alibaba close to porting Android to RISC-V [Internet]. Poole: Electropages; 2022 Apr 5 [cited 2022 Jul 5]. Available from: https://www.electropages.com/blog/2022/05/alibaba-close-porting-android-risc-v.

[10] Martin D. One of the first RISC-V laptops may ship in September, has an NFT hook [Internet]. London: The Register; 2022 Jul 1 [cited 2022 Jul 5].

Available from: https://www.theregister.com/2022/07/01/riscv_roma_laptop/.
[11] Analyzing the RISC-V CPU market for SIP, SoCs, AI and design starts [Internet]. Phoenix: Semico; 2021 Nov 17 [cited 2022 Jul 5]. Available from: https://semico.com/content/analyzing-risc-v-cpu-market-sip-socs-ai-and-design-starts.
[12] Freund K. Esperanto launches AI accelerator with over 1000 RISC-V cores [Internet]. Jersey City: Forbes; 2021 Aug 24 [cited 2022 Jul 5]. Available from: https://www.forbes.com/sites/karlfreund/2021/08/24/esperanto-launches-with-1000-core-risc-v-ai-accelerator/?sh=128f2b5bbded.
[13] Martin D. Samsung, others test drive Esperanto's 1000-core RISC-V AI chip [Internet]. London: The Register; 2022 Apr 22 [cited 2022 Jul 5]. Available from: https://www.theregister.com/2022/04/22/samsung_esperanto_riscv/.
[14] Weiss T. Ceremorphic touts its HPC/AI silicon technology as it exits stealth [Internet]. San Diego: HPC Wire; 2022 Jan 25 [cited 2022 Jul 5]. Available from: https://www.hpcwire.com/2022/01/25/ceremorphic-exits-stealth-touts-hpc-ai-silicon-technology/.
[15] Cherney MA. The newest autonomous driving chip from Intel's Mobileye doesn't have any of Intel's core tech [Internet]. San Francisco: Protocol; 2022 Jan 4 [cited 2022 Jul 5]. Available from: https://www.protocol.com/bulletins/intel-mobileye-eyeq-autonomous-driving.
[16] Weiss TR. Kneron unveils its first RISC-V SoC built for autonomous, assisted driving [Internet]. San Diego: Enterprise AI; 2021 Nov 3 [cited 2022 Jul 5]. Available from: https://www.enterpriseai.news/2021/11/03/kneron-unveils-its-first-risc-v-soc-built-for-autonomous-assisted-driving/.
[17] Khalili J. Will Intel abandon x86 for RISC-V for its next-gen supercomputing chips? [Internet]. New York City: TechRadar; 2022 Jun 5 [cited 2022 Jul 5]. Available from: https://www.techradar.com/news/will-intel-abandon-x86-for-risc-v-for-its-next-gen-supercomputing-chips.
[18] Shilov A. Researchers benchmark experimental RISC-V supercomputer [Internet]. New York City: Tom's Hardware; 2022 Jun 11 [cited 2022 Jul 5]. Available from: https://www.tomshardware.com/news/researchers-benchmark-experimental-risc-v-supercomputer.