

## Views &amp; Comments

## Thoughts on China's Integrated Circuit Chip Manufacturing in the Post-Moore Era



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## 1. Background

As one of the fundamental and core industries of modern information technology, the integrated circuit (IC) is a basic and leading industry that is closely related to overall global economic and social development. The global semiconductor industry is poised for a decade of growth and is projected to become a trillion-dollar industry by 2030 (Fig. 1 [1]). Technological level and industrial scale are important indicators for evaluating the degree of modernization and comprehensive national strength of a country or region. Hailed as the “industrial food” for a country, IC is the foundation for cultivating and developing strategic emerging industries and promoting the deep integration of informatization and industrialization. Demand for both cutting-edge chips and high-reliability chips continues to be strong in applications deployed throughout the field, from Industry 4.0 to automotive electronics, artificial intelligence, and so forth. As the focus of current international competition, IC also plays a broad and key role in promoting national economic development and social progress, improving people's living standards, and ensuring national security. The current competition is not related to a certain technology node or single specific technology. Rather, this core competitiveness is the overall strength of the IC industry chain and relies on the ability to track the dynamic targets of industrial development, which fully depends on the support of the global high-end basic industry.

## 2. Features of the post-Moore era

In a discussion of this topic, it is necessary to start from an understanding of Moore's law, which was proposed by Gordon Moore, one of the founders of Intel. In the journal *Electronics* in 1965, Moore predicted that the complexity of IC would double annually at the lowest component cost [2]. Ten years later, at the 1975 IEEE International Electron Devices Meeting (IEDM), Gordon Moore proposed that the transistor density (TrD) on a chip could be doubled every 2–3 years [3]. In the subsequent 40 years, micro-processor development basically followed this pace. However, memory chip density has been developed at a relatively more aggressive pace, doubling every 18 months. Moore himself believed that the cost of technological development would be dif-

ficult to maintain by 2005; however, from a technical perspective, technological development can continue according to Moore's law until 2025.

In a discussion on technological development, Paul Otellini, the former president of Intel, commented that the Research and Development (R&D) goal of Intel is not only to meet these important performance parameters but also to meet the parameters of power consumption per watt. Thus, the concept of “performance per watt” was proposed [4]. The reality is that, after the development of the 28 nm technology node, it seems difficult for the industry to double the TrD while maintaining the cost per unit area. In future technological development, it is necessary to balance among performance, power consumption, and cost. That is, if the application target mainly requires high performance, it is necessary to abandon the pursuit of power consumption and cost. Conversely, simply considering cost reduction will inevitably result in tradeoffs in both power consumption and performance. These three components cannot be updated every-two years under the framework of Moore's law. Therefore, it can be considered that 28 nm technology generation presents the end of Moore's law, and 20 nm technology generation creates the post-Moore era.

Fig. 2 [5] shows that the TrD has been improved to varying degrees in each new generation of technology nodes, with the TrD of Intel nearly doubling. Taiwan Semiconductor Manufacturing Company (TSMC) and Intel define TrD differently, so their progress in TrD cannot be compared in a true mean; it can only be compared with their own technological generation, which is far from the goal of “double the density” of transistors in new-generation chips every-two years, as proposed by Moore's law. The relative cost per unit of TSMC is also shown in Fig. 3 [6], where the cost slope scales down from the 20 nm technology node. Furthermore, Fig. 4 [7] shows the 2020 China IC revenue share of different technology nodes.

The post-Moore era has the following five characteristics: ① The technical direction is still under exploration; ② the (transistor) line width is no longer the only parameter to deliberately pursue; ③ there is a wide range of applications, both all around the world and in all parts of daily life; ④ there is market fragmentation, with no obvious monopoly; and ⑤ R&D expenditures are relatively low.

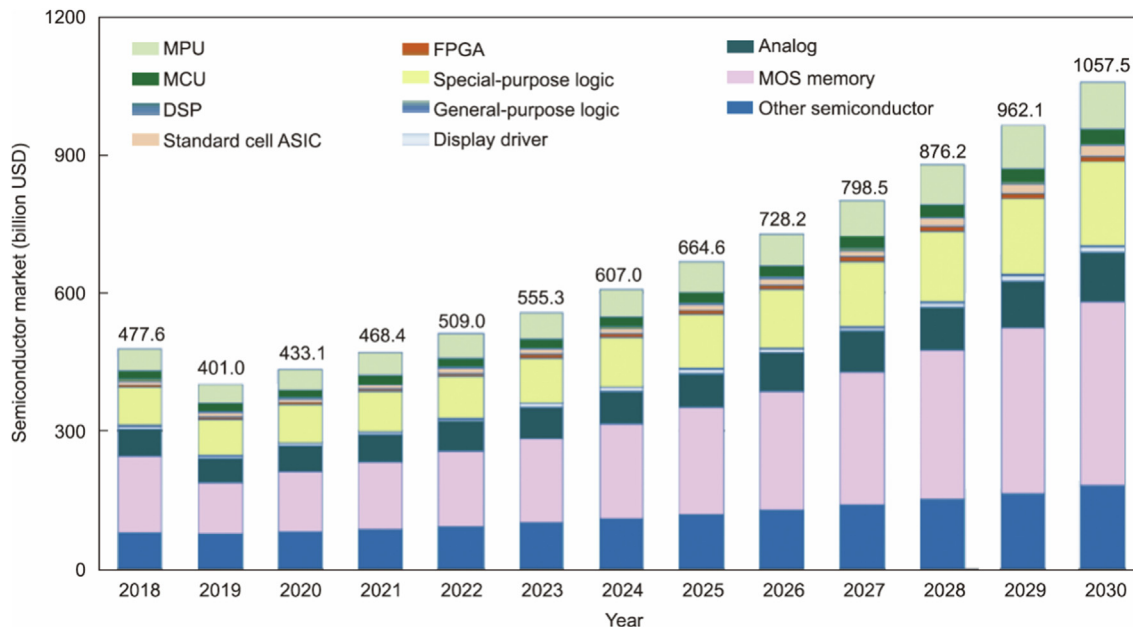


Fig. 1. Trends of the global semiconductor market by product. Semiconductor market will be 1 trillion USD in 2030. The data are from Semiconductor Equipment and Materials International (SEMI) [1]. MPU: microprocessor unit; MCU: microcontroller unit; DSP: digital signal processing; ASIC: application specific integrated circuit; FPGA: field programmable gate array; MOS: metal-oxide-semiconductor.

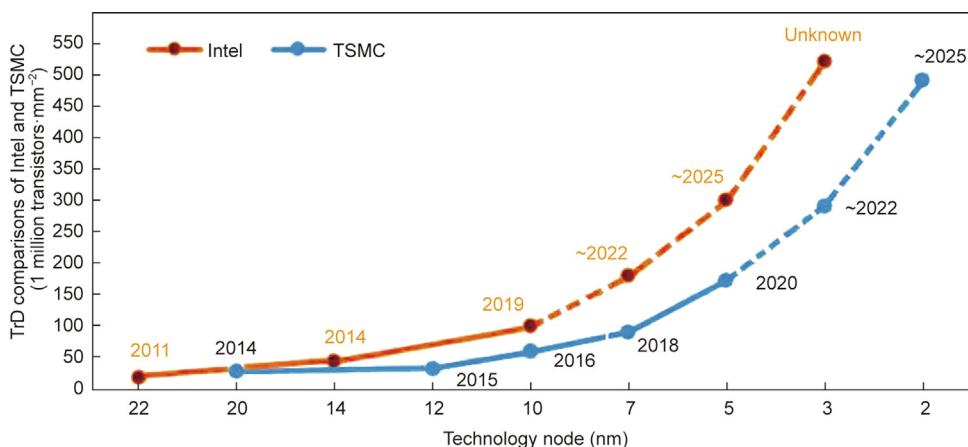


Fig. 2. TrD versus technology node of the leading chip foundries, Intel and TSMC [5]. TSMC: Taiwan Semiconductor Manufacturing Company.

Within Moore’s era, the size of technology shrinks every-two years, with innovative applications being based on this conception. This is an example of what is known as “inertial thinking” (e.g., including applications, everybody is moving in one direction). Conversely, in the post-Moore era, innovation is unlimited and everyone innovates in different directions based on their own experience. With divergent thinking, ideas compete with one another, and there are no clear winners or losers. For example, in quantum computing and neuromorphic computing, a new industry pattern will probably emerge. How many of the current top ten innovations will survive? This is almost impossible to predict.

Moore’s law is not a “real” law discovered through scientific research. Rather, it is an empirical law explaining the relationship between technological research and industry development. The essence of Moore’s law is the unification of technological monopoly and technological competitiveness. Moore’s law is also the result of compromise between technology and capital in the development of industrial technology.

### 3. Challenges and opportunities in the post-Moore era

Given the characteristics of the post-Moore era mentioned above, there will be five related development opportunities for China in the post-Moore era: ① There will be broad room for technological innovation; ② equipment will be less expensive, and the conditions for other technological development will be less harsh; ③ there will be a huge market space and significantly lower difficulty in recovering investment; ④ it will be easy for innovation-oriented small and medium-sized enterprises (SMEs) to survive and grow in the Shanghai Stock Exchange (SSE) sci-tech innovation board (STAR market); and ⑤ it will be easy to develop products, and R&D team and funding requirements will not be unattainable. Those who have a good grasp of these opportunities can effectively narrow the gap between China and the world’s industrial technology level.

From a macro perspective, the challenges in the post-Moore era mainly come from the two aspects of technology and society. The

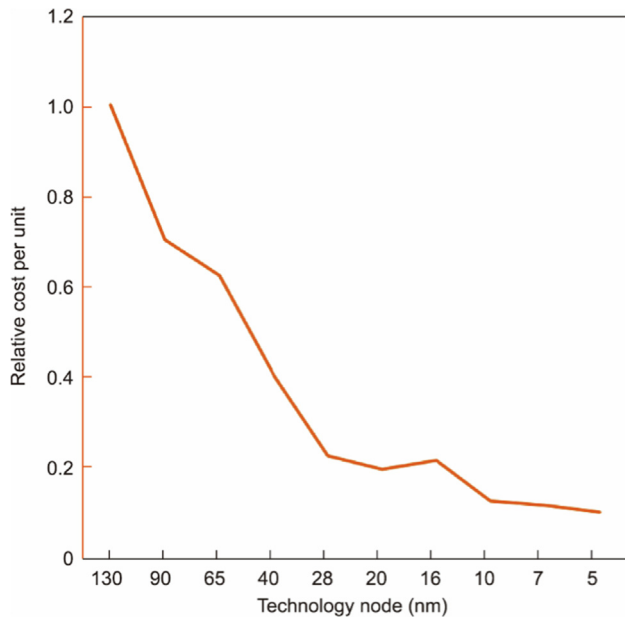


Fig. 3. Relative cost per unit of TSMC technology nodes [6].

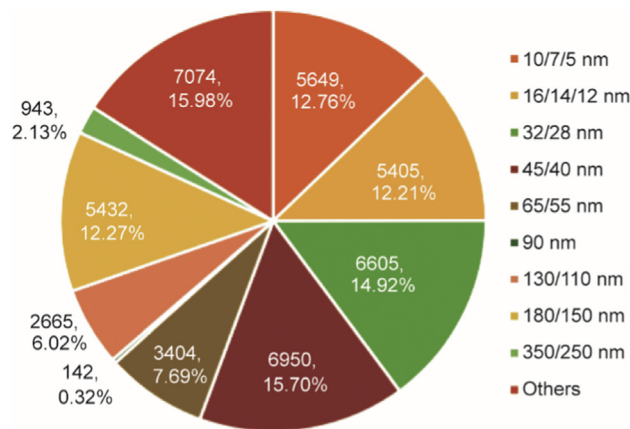


Fig. 4. China IC product revenue by technology nodes [7]. The unit is million dollars.

former is a bottleneck encountered by countries all over the world at present, while the latter is an ecological construction of industry under the unique deglobalization environment faced by the rising China.

### 3.1. Technical challenges in the post-Moore era

Due to the rapidly increasing barriers to technology R&D investment in the post-Moore era, only Intel, Samsung, and TSMC are still investing heavily in the development of 5 nm and beyond technology nodes, and have reached the goal of 5/7 nm manufacturing. The Semiconductor Manufacturing International Corporation (SMIC) in the Chinese mainland also announced three years ago that the 14 nm technology node had achieved the “customer introduction” stage. The equipment used in the global high-end chip fabrication process below 14 nm is basically made in the United States and Japan, while the lithography machine is made in the Netherlands. The Dutch corporation ASML’s most high-end extreme ultraviolet (EUV) lithography machine is supported by

more than 5000 top component material suppliers in various countries around the world, with the Netherlands’ native technology accounting for about 30%. More specifically, the core light source adopts US technology, the optical system adopts German technology, and most of the materials come from Japan.

The trend of advanced chip manufacturing technology in the post-Moore era is a hybrid of extremely small-scale and super large-scale projects. The extremely small scale means that the transistor is physically smaller than 10 nm (the diameter of a hair is about 10 000 nm). The accuracy is less than 1 nm in some critical dimensions. The super large scale means that hundreds of billions of transistors, hundreds of billions of vias or contacts, and tens of thousands of kilometer-long trenches that are just a couple of nanometers wide need to be simultaneously fabricated on a large silicon wafer with a diameter of 300 mm, with an error of less than a nanometer. This minimality has almost reached the physical limit of human modern manufacturing, and the super large scale embodies the highest level of contemporary system engineering [8].

Three key challenges are presented by IC manufacturing process technology: precise pattern transfer, material and process technology, and yield improvement and cost control.

#### 3.1.1. Precise pattern transfer

The first challenge is a fundamental one: precise pattern transfer, which mainly refers to the transfer of the design pattern onto a silicon wafer through a combination of lithography and etching. Local material modification achieved by ion implantation also needs to be defined by lithography. The lithography technology determines the process technology node. For example, below 130 nm (or 0.13 μm), it is necessary to use ArF, which has a wavelength of 193 nm, to define the etching area for the subsequent etching process. This dry ArF lithography supports the three generations of 130, 90, and 65 nm nodes. When the technology evolves to the 45/40 nm technology node, it is necessary to adopt immersion ArF lithography, which supports the 45/40 and 32/28 nm technology nodes. Starting from 22/20 nm and including 16/14, 10, and 7 nm technology nodes, the fourth-generation technology is supported by the multiple exposure technology of immersion ArF. Since the beginning of 5.0 nm technology, EUV lithography, which has a wavelength of 13.5 nm, has become the mainstream of the industry. Theoretically, it is possible to implement chip manufacturing at the 5 nm technology node without EUV lithography—that is, it is possible to achieve pattern transfer through multiple exposure technology. However, due to yield and cost considerations, EUV lithography technology is used in the mainstream industry.

Lithography is the basis of pattern transfer. After lithography is completed, etching is used to transfer the lithographic pattern onto the silicon. Currently, the industry widely adopts plasma etching, in which the area defined by lithography can be engraved on silicon according to the anisotropic characteristics of the plasma. The etching target, which is only tens of nanometers wide, is extremely sensitive to the plasma parameters. Therefore, optimal control of the plasma parameters has become the focus of etching process technology.

#### 3.1.2. Material and process technology

The second key challenge lies in new material and process technology. In the early development of IC chip technology, the role of materials was not given sufficient attention. At the start of the 21 century, when the technology node developed to the 130 nm technology generation, the role of materials began to emerge, mainly because the previously used aluminum wire was replaced with copper wire for back-end interconnection. At the same time, the traditional back-end medium, silicon oxide, gave way to the low-κ (where κ is the permittivity) fluorosilicate glass (FSG) material.

Although copper is not a newly discovered material, the application of copper to the IC chip introduced great challenges. The major reason was that copper is uniquely non-volatile, making it necessary to innovate the processing technology subversively so that a copper wire pattern could be applied to the back-end of the chip. For this reason, a new copper-related technology called “dual Damascene” came into being. This technology works by forming nano-scale trenches or “vias” through pattern transfer and filling them with copper to form copper wires or copper pillars. This technology is analogous to the ancient Chinese cloisonné technique, in which a pattern is made on porcelain, filled with copper, and then polished to form a beautiful figure. Due to the high electron mobility and diffusivity of copper, a thin film must be prepared to block the migration and diffusion of copper before the copper is filled, and a copper film must be prepared as a seed layer for electroplating in order to implement the electroplating process. However, the technical requirements for the preparation of these films are particularly demanding.

With the advent of 65 nm technology generation, as SiGe was adopted, strained silicon devices began to be mass produced; later, the high- $\kappa$  metal gate technique, which was part of the 45 nm technology, began to enter mass production. It is precisely due to the support from these new materials and new techniques that the positive channel metal-oxide-semiconductor (PMOS) performance for the 32 nm technology node has been improved by 70%. Only professionals with solid material knowledge could successfully develop these new film process technologies. Looking back at the development trajectory of IC chip technology in accordance with Moore's law, it is not difficult to see that the R&D achievements of new materials have been the core pillar of Moore's law for 50 years.

Obviously, in the process of technological development in the post-Moore era, the core role of new materials will be embodied more prominently. Taking the last ten years of chip technology development as an example, from high- $\kappa$  metal gate dielectrics to ultra-low- $\kappa$  materials, and from strained silicon to metal silicides, all are the results of new materials and new process technology development. Recently, leading chip companies have adopted bismuth as a new material for the development of 1 nm technology, which has significantly improved the performance. Therefore, it can be seen that new material technology is at the core of technological development in the chip manufacturing industry.

### 3.1.3. Yield improvement and cost control

The ultimate challenge of the industry is yield improvement and cost control. Yield and cost go hand in hand as the eternal themes of industrial technology development. In the post-Moore era, with the shrinking of feature sizes, various random events pose increasing threats to quality control and increasing challenges to yield improvement. Nano-level statistical fluctuation, which did not affect the yield before, may become a great threat to the yield of the production line in the post-Moore era.

For example, the average number of photons to which a small amount of photoresist is exposed corresponds to the required exposure dose. If a certain amount of photoresist is exposed to a high number of photons, the relative random variation will be small. The photon shot noise refers to the change in the number of photons in the lithographic process. EUV photons carry 14 times more energy than 193 nm photons. Thus, the same exposure dose has 14 times fewer photons. The smaller the number of photons, the higher the photon shot noise. In the example of the industrial lithography process, the light energy flux is about  $15 \text{ mJ}\cdot\text{cm}^{-2}$ , and the photon flux in ArF-based 193 nm lithography is about  $145 \text{ photons}\cdot\text{nm}^{-2}$ . However, the photon flux in the EUV lithography process with the same energy is only about  $10 \text{ photons}\cdot\text{nm}^{-2}$ . One photon error can cause a 10% process error, which severely

affects the line edge roughness (LER) in the lithography process. In addition, in the ion implantation, only a few hundred ions are modulated by the threshold voltage, and the fluctuation of several ion fluxes may cause unacceptable yield loss to the product. To address these problems, precise process control and yield improvement technology are required [9].

From the perspective of the industrial structure and characteristics, yield improvement on a production line is usually related to the key process parameters of the entire production line. Moreover, these process parameters are the most sensitive core technologies on the production line of chip manufacturers, and the intellectual property rights are usually preserved in the form of “know-how.” The technical personnel of external research institutes and universities cannot obtain these core parameters. Therefore, many scientific problems in yield improvement cannot be solved through cooperation among industry, universities, and other research institutes, and must instead be solved by the enterprise in question, based on its limited technical expertise. Such solutions usually yield half the result with twice the effort. Only in a production line equipped with a complete set of techniques can it be possible for scientific and technical personnel to collect key process parameters through specially designed test keys and to trace the source of defects through a scientific mathematical analysis model, thereby solving the issue decreasing the yield. Therefore, it is commonly acknowledged that it is impossible to systematically develop yield improvement technology on a public platform without an entire process flow.

The fundamental challenge in the development of manufacturing techniques for IC is precise pattern transfer; the core challenge is the development of new materials and new process techniques; and the ultimate challenge is yield improvement and cost control. Dealing with each challenge is estimated to require one third of the total R&D investment resources. These three challenges must be addressed on a technical platform equipped with an entire process flow.

### 3.2. The post-Moore ecosystem under the anti-globalization environment

The current international situation is full of challenges and opportunities. Some countries have repeatedly abused tariff barriers and national-security provisions to block some leading high-tech companies from a national interest perspective, regardless of fundamental World Trade Organization (WTO) regulations. At present, the strategic power game among the global powers is primarily embodied in high-tech development, especially concentrated on the technical level of IC manufacturing.

There was a period of time in the past when China upheld the technical idea of introducing, digesting, and absorbing ideas from outside of the country due to the impact of an idea that was formed under the conditions of a pure market economy—namely, that it is better to buy than to produce, and it is better to rent than to buy. However, if the introduction of new technology to China is blocked by foreign interests in the future, it will be impossible to digest and absorb such technologies. In the past, China lacked sufficient determination for the policy of self-reliance on IC industry. As a result, R&D projects are often interrupted, causing us to fall even more short of our advanced international counterparts.

In addition, China has not yet paid enough attention to industry-oriented high-tech cultural construction. Over the past decades of scientific and technological development, from R&D project initiation to project implementation, industry leadership has not been consistently implemented. For many years, the separation of the IC industry from education, research, and development has not been fundamentally resolved. Taking chip manufacturing as an example, the first single-crystal silicon was produced in China



in 1958; then, the first silicon-based IC chip was developed in 1965. The gap between China, the United States, and Japan at that time was not significant, such that the three nations were roughly on the same starting line [4]. However, industrialization in China slowed down in the subsequent 30 years, and it was not until 1988 that China became capable of producing 100 million ICs annually—about 20 years behind the United States and Japan. Thus far, the “chip shortage” in the IC industry has proved that the industry-led development path of “research is the means, industry is the goal, and production capacity is the king” must be advocated and adhered to.

In the current chaotic global economic environment, the security of the supply chain and industry chain is disrupted, and the idea of continuing to solely pursue advanced technology is questionable. The development of a complete set of advanced technology requires massive resources. Taking 28 nm node manufacturing technology as an example, the development of a complete set of process flow technologies takes about 1 billion USD and thousands of outstanding engineers and technicians. Moreover, it takes about four years to reach the mass-production level. In particular, the subsequent return on investment (ROI) will be even more difficult under the squeeze of the world market. For the 14 nm technology node, the development of a complete set of advanced technologies requires twice the resources of the 28 nm technology node, and the return on capital is even more unreachable. Without the support of market-related economic levers, R&D funds from the government alone cannot maintain sustainable advanced technological development.

The future technology development route requires a clear purpose and means. An advanced production line can be set up for the main purpose of promoting local equipment and material companies to develop, thereby establishing a local industrial chain. Hence, it is of more practical significance to establish a basically controllable complete set of manufacturing technology by retreating in order to advance. That is, in addition to investing appropriate resources in order to continue to progress the R&D of advanced technology, the most urgent thing is to invest the main resources to carry out the R&D of the localization of existing advanced techniques, as well as technology R&D and the capacity expansion of relatively mature technologies. It is not necessary for every R&D project to be fully autonomous and controllable, as long as it is basically controllable. The establishment of a basically controllable 55 nm production line is of far greater significance than the establishment of a 14 nm production line that relies entirely on imported equipment and materials. The current competition among leading countries and regions is obviously not only within a certain advanced technology node but covers the overall industry chain.

There is a similar development idea for the development of basic equipment technology. Taking the lithography machine as an example, we may not have to follow the existing technical route in order to catch up with the development of the most high-end EUV lithography machine. Instead, we should focus on original innovation in lithography technology and strive to explore fundamental alternative technologies so as to manufacture domestic lithography machines equipped with our own core technology. If we just follow the technical route set by the world's leading companies, it may be difficult to catch up with the world's advanced lithography technology applicable to the industry. At present, the most advanced EUV lithography machine is assembled from more than 100 000 parts provided by more than 5 000 top global parts suppliers. The entire EUV lithography machine is equipped with US light source technology, German optical technology, a British vacuum system, Japanese material technology, and other advanced techniques from other countries around the world. Apparently, it is impractical to make an industrially applicable advanced lithogra-

phy machine by relying on a single country or region's own strength. As the IC market and industry develop well domestically, we might as well take advantage of this opportunity to formulate various preferential policies to support lithography machine companies in achieving industrialized development based on the major national technical achievement (i.e., the 193 nm ArF lithography machine) so that, in the coming years, the production capacity of domestic lithography machines can be enhanced in order to partly meet domestic needs for the construction of new chip manufacturing production lines. An enterprise must first grow bigger in order to grow stronger.

Fig. 5 [10] shows the 2018 semiconductor sales along the value chain for major regions. It is very clear that no local market or company possesses all the capabilities required for end-to-end semiconductor design and manufacturing. Therefore, we must remain clear- and open-minded while “focusing on national interests,” attract top global talents, and try our best to cooperate with companies that adhere to the idea of globalization and advanced technologies. We should encourage inviting foreign companies to China to promote their localization and pushing local companies to expand toward globalization. Let us give full play to China's huge market advantages in order to actively carry out a dual-circulation development route. It is helpful to follow the laws of economic development to make an increasing number of connections in the business community, and China will definitely have the opportunity to implement external circulation. All attempts to violate the laws of economic development and to set up business alliances through ideology are doomed to fail.

#### 4. Suggestion

Accordingly, we provide four insights and recommendations on China's chip manufacturing:

(1) **Make full use of the achievements from major national projects to support the development of specialty technologies and the related industry chains.** We can speed up our development of IC technology in order to catch up with industry leaders in the post-Moore era, as the advancement of process technology slows down and there is plenty of room for marketing and product technology innovation. Products fabricated at nodes 14 nm and above account for 83% of the global market share. If China could put more than half of the manufacturing capacity of these specialty technologies under its own control, we would be able to obtain more impact and power over the industry to a certain extent. Therefore, China must provide stronger support for the development of mainstream specialty technologies while tracking the R&D trends of cutting-edge technologies. Relying on our advantages in economy scale, we can strive to attain more power in the international market within the huge field of the chip manufacturing industry. We must also speed up the localization of China's core industry chain, including the equipment, materials, and core components developed with the currently available process technology. A sound and controllable industry chain will help to put us in an invincible position in the competition among leading powers.

(2) **Adhere to an industry-oriented technology roadmap.** IC technology development did not start late in the Chinese mainland (the first single-crystal silicon was invented in 1958 and the first IC chip was developed in 1965), and there is a much larger population of IC industry practitioners in the Chinese mainland than in the Republic of Korea and the Taiwan region. But why has the industry developed in an unsatisfactory manner in the Chinese mainland till now? Looking back at the development history of China's National Integrated Circuit Industry Development Promotion Outline, which started more than seven years ago, even with the colossal

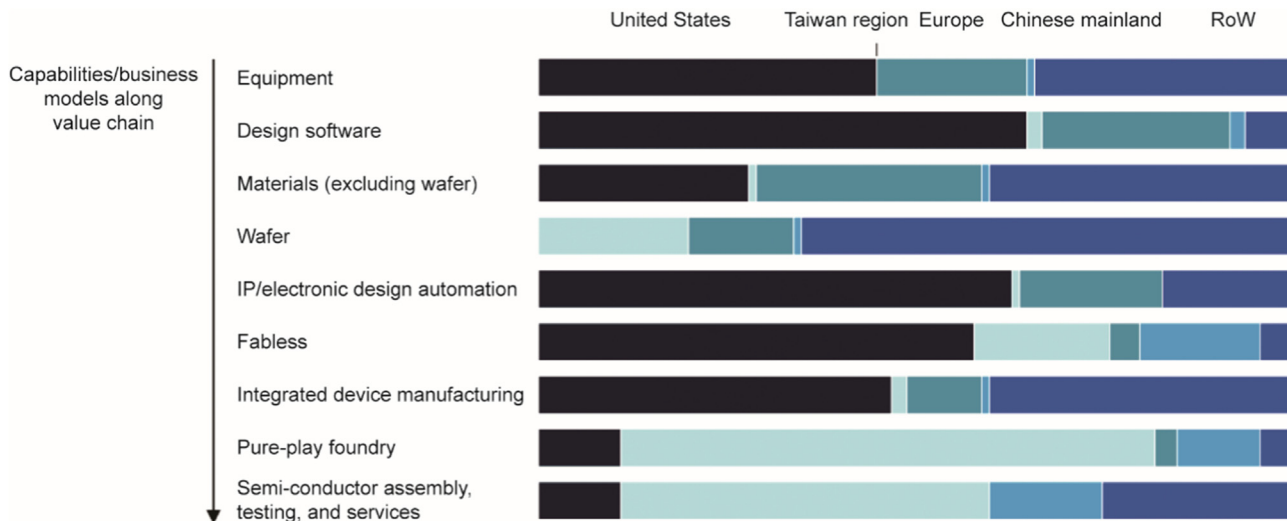


Fig. 5. 2018 semiconductor sales along the value chain (% share) [10]. IP: intellectual property; RoW: the rest of the world.

investments that have been made, China's semiconductor market has not decreased its dependence on foreign countries; instead, the ratio of imports from the global semiconductor market has increased from 64.8% to 82.2% over the past seven years. The main reason is that the investment is relatively scattered and far from enough; moreover, there is a critical shortage of world-class talents in the domestic industry. The development of leading companies in China is still far from keeping up with the pace of global industrial development. On a fundamental level, sufficient attention must be paid to the weaknesses of industry-led technological culture, which is a problem that has plagued China's development process for decades.

(3) **Adhere to a path of self-reliance and opening up to the outside world.** China still has a long way to go to develop IC chips. There are no existing corners for us to cut, so the development path of China's chip industry is destined to be full of hardships. In particular, the chip manufacturing process, which has been developed on the basis of globalization, will inevitably present severe and long-term challenges. Although the road to globalization is not smooth, it is still necessary to promote the internationalization of Chinese enterprises and the localization of foreign enterprises with the aid of a dual-circulation model. We also need to learn advanced technology from other nations and recruit elites with an open mind. Among these steps, the localization of the world's leading intellectual property (IP) company, ARM, and other large international companies is a valuable example worthy of study and reference.

(4) **Establish an integrated public technology platform for design and manufacturing with complete mainstream process flow capabilities.** At present, China still lacks a truly neutral industry-education-integrated and science-education-integrated high-end public R&D platform where a complete set of chip manufacturing technologies can be developed. A public platform would use typical products as carriers in order to carry out collaborative innovation among industry, universities, and other research institutes. Such a platform would have four main functions: ① It would efficiently support the product tape-out verification of innovative design companies, shorten the research and development cycle, and enable new products to enter the market as soon as possible; ② it would provide process verification tape-outs for equipment and material manufacturers, allowing them to promote the construction of all links in the industry chain; ③ it would create a new industry talent-training model in the form of the industry-education integration of design and manufacturing training bases for

domestic colleges and universities; and ④ it would support enterprises in developing common technologies for the mass production of chips (e.g., yield improvement for a complete set of techniques, optimization of production process flow, virtual production line construction, etc.). In particular, it is necessary to help enterprises to overcome technical difficulties that cannot be solved by a single company. It is also necessary to remain open to communication with global companies regarding platform construction, and to cultivate leading innovative talents and interdisciplinary engineering talents who have forward-looking vision and can lead future development.

## 5. Conclusions

Various technological innovations are emerging one after another in the IC industry in the post-Moore era. However, there is still a lack of a clear mainstream silicon-based technology trend. Various disruptive technologies are also dazzling. Nevertheless, we must remain clear-headed and stick to mainstream technology development. We can take one step back and then two steps forward in order to appropriately slow down investment in advanced technological development to some extent and increase investment in large-scale and wide-ranging specialty technological development and controllable industry chain construction. Any cutting-edge disruptive technology may become an industrial technology in ten years from now. While paying attention to disruptive technology, we must have sufficient support for the development of mainstream industrial technologies, which is the foundation of China's industrial development and necessary for the future survival of this industry.

Since the IC industry covers a wide range of fields, its industry chain is extremely long, and our limited vision will inevitably lead to some deficiencies. We sincerely welcome readers' criticism, corrections, and suggestions.

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