450 mm Silicon Wafers Are Imperative for Moore's Law but maybe Postponed

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Fifty years ago Mr. Moore wrote a paper for *Electronic News* on cramming more components onto the microchips which leading to the prestigious "Moore's law" he could not utter for the first twenty years. And now Moore's law becomes a miracle in human history as Intel chief executive Brain Krzanich recently pointed out that if a 1971 Volkswagen Beetle had advanced at the same pace, it would be able to drive at speeds up to 300 000 miles per hour and cost about 4 cents.

Twenty years from now, a 20-year vision probably is the limit for gauging the distant future in the rapid development scenario; if we desire to take the advantage of Moore's law, one of the adequate approaches is to introduce 450 mm silicon wafers for 10 nm technology node and beyond. Mr. Moore saw wafers growing, as early as in 1965, ever large as a way to keep the device cost down. Historically, each wafer size transition has been technically more challenging as complexity increases. The lesson learned from 300 mm silicon wafers indicates it is a necessity for the technology advances, business modal, economy and market dynamics, and industry collaboration in all aspects to come into play in the development of 450 mm crystal growth, wafering technology and the related equipment.

Siltronic AG first reported the successful growth of a 400 mm silicon ingot in 1995. Following that, in 1996 the Japan Key Technology Center and seven Japanese silicon wafer companies established Super Silicon Crystal Research Institute (SSi) which had spent five years to develop 400 mm crystal growth, wafering and epitaxial technologies in three labs. The technical results achieved by SSi are valuable, yet not fully meet the cost/performance requirements of the next generation integrated circuits (ICs). General Research Institute for Nonferrous Metals (GRINM) in Beijing also grew a 400 mm single silicon crystal in 1999 with a 28 in (1 in = 2.54 cm) hot zone.

Semiconductor Industry Association (SIA) in the year 2000 issued the International Technology Roadmap of Semiconductors (ITRS) in which the next generation starting materials are 450 mm silicon wafers not 400 mm. Since then, there had been many debates: Intel, Samsung and TSMC had been urgent about the 450 mm equipment and materials development whereas AMD and other device makers had opposed this transition. Only in recent years, consensus on 450 mm transition has been reached. ICs technology developments, hence, have been pushed forward by global cooperation instead of individual manufacturers. There are very regular meetings of Global 450 Consortium (G450C), the European 450 mm Equipment and Materials Initiative (EEMI450) and the Metro450 consortium (based in Israel) which have proven highly constructive and all three groups take the results from the others without repeating any measurements. Apart from Semiconductor Materials Technology Consortium (SEMATECH) and Semiconductor Equipment and Materials International (SEMI)'s programs, global industry chain cooperation has focused on nano-scaled ICs processing technology and equipment which effectively impact the 450 mm wafer technological progress and application. The appropriate timing for 450 mm transition depends on the economic justification of its better cost/performance over 300 mm. Last year there were signs of pausing development on 450 mm for G450C partners. The Taiwan Semiconductor Manufacturing Company (TSMC) has made public for some time: They do not

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expect 450 mm until 2018. The big players perhaps are waiting for the new creative applications such as the Internet of Things, Google's gigabit fiber, Apple's disruptive technologies to increase the IC demand which will ultimately be the direction required for all to benefit.

Update of G450C's work is promising, on April 16, 2015, the installation of the world's first ever 450 mm immersion scanner began at the SUNY Polytechnic Institute's Albany NanoTech Complex. Developed by Nikon Corporation, this first of its kind tool would accelerate the development of the next generation microchips. Meanwhile, in May of 2015, Mipox released a polishing machine for 450 mm wafers equipped with a new polishing head and a polishing technology based on many years of accumulated knowledge. The machine achieves high efficiency of polishing process at over double speed with newly-developed polishing films and the method for the top edge of wafer periphery. Polishing service is to begin in July 2015.

The technical challenges associated with the introduction of 450 mm silicon wafers include crystal furnace and hot zone designs, neck issues, wafer thickness and flatness, wafer geometry and edge shape, mechanical processes, impurities and defect control, and so on. Research work has been conducted in advanced crystal growth to ensure crystal quality, uniformity and yield as well as control of crystal originated pits (COPs). At the present time there do not appear to be any fundamental barriers to convert 450 mm crystals to wafers. The wire saw can be scaled to cut 450 mm ingots, however the increased drag on the wire may limit the wire diameter, impact the kerf loss and affect the total thickness variation (TTV) of the as-cut wafers. The 450 mm wafers will possess the much more tight uniformity of doping and thickness, less defect density and stringent local flatness SFQR (i.e., site flatness front least-squares range). In order to obtain the better quality substrates, subtle control of contamination and interaction between defects and impurities has to be taken into account.

Computer simulations have been the powerful and cost effective tool that can shorten the experimental time and reduce the energy consumption and usage of highly purified materials such as polysilicon, quartz crucibles, and graphite heaters. Numerical analyses indicate that as the minimum features shrink, the size of "killer" defects also decreases and uniform material distribution on 450 mm wafers is critical to process yield and success. In addition, a detailed model must be developed in order to solve the economic issue which must represent the real situation for the materials in the supply chain, since 450 mm wafers require re-optimizing materials' mixing and delivery.

For volume production of 450 mm wafers, the productivity and cost of crystal growth need to be emphasized. It has been suggested that the charge size and the crucible diameter should be about 1000 kg and 40–44 in, respectively. To overcome the technology difficulties for 450 mm crystal growth with low cost, GRINM fabricated a 450 mm silicon single crystal in 2002 and has been manufacturing ingots on a production scale since 2013 for IC equipment parts. The Silicon United Manufacturing Company (SUMCO) reported that it has been ready to provide the test and production of 450 mm wafers.

The transition to larger wafer sizes always faces the challenges. If 450 mm original equipment manufacturers (OEMs), target 10 nm and beyond, significant process changes will have occurred and some 10 nm tools may need further modifications to meet 7 nm and 5 nm expectations. The workable solution is that the transistor channels may use higher mobility materials such as Ge or InGaAs rather than Si. Nevertheless, the heteroepitaxy may add complexity to the large Si substrates.

The development of 450 mm standards has been taken as a key activity of promoting 450 mm transition. After the first 450 mm standard was generated in 2008, SEMI has published 19 standards and 13 standards in the pipeline. These standards specify the requirement for 450 mm polished and epitaxial wafers, and provide the guidelines for geometry measurement and surface inspection. The 450 mm wafer thickness, for example, will be 925 μm in lieu of 825 μm suggested previously. 450 mm wafer notch can be centered on <110> or <100> axis whereas the notchless wafer standard has recently been approved. Today, the specification requirements for 450 mm wafers are much more extensive than those of previous smaller diameters. Standardized parameters include edge profile, warp, conductivity, dopants, and surface conditions, and SEMI standard task force has been working hard on developing the new standards for 450 mm wafers.

The roadmap for 10 nm, 7 nm, and 5 nm technology nodes will be discussed in the coming 2015 SEMICON/WEST trade show, where the Semiconductor Technology Symposium (STS) technical program will explore the resistance-capacitance management, integration, and high-volume and low-cost manufacturing challenges. The story is certainly not like what someone imagines that silicon is out of date. In contrast, nano-silicon and Si^{28} have the potential to develop the solid-state quantum computer devices, and 450 mm silicon wafers combining with high-mobility channel materials, high dielectric-constant (*k*) materials, carbon nanotube (CNT), graphene, polymer, and bio-based materials will still be the competitive candidates to pave the way to 5 nm technology. The major breakthrough in lithography and key equipment should be accomplished within a few years, which is partially contingent upon the game-playing among equipment companies and IC manufacturers. Furthermore, the synergy that comes from combining top-down with bottom-up technological approaches will continue to change our lives and bring many benefits to modern society—as well as providing an enormous impetus to the new industrial revolution.