Engineering 22 (2023) 125–140

Contents lists available at ScienceDirect

Engineering

journal homepage: www.elsevier.com/locate/eng

Research
Wireless Communications—Article

A 39 GHz Dual-Channel Transceiver Chipset with an Advanced LTCC Package for 5G Multi-Beam MIMO Systems

Yiming Yu [a], Zhilin Chen [a], Chenxi Zhao [a], Huihua Liu [a], Yunqiu Wu [a], Wen-Yan Yin [b], Kai Kang [a,*]

[a] School of Electronic Science and Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China
[b] College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310058, China

ARTICLE INFO

Article history:
Received 9 November 2021
Revised 18 January 2022
Accepted 17 April 2022
Available online 27 August 2022

Keywords:
5G
Multi-beam
Multi-input multi-output
Millimeter-wave
Transceiver
Wireless communication

ABSTRACT

This article presents a 39 GHz transceiver front-end chipset for 5G multi-input multi-output (MIMO) applications. Each chip includes two variable-gain frequency-conversion channels and can support two simultaneous independent beams, and the chips also integrate a local-oscillator chain and digital module for multi-chip extension and gain-state control. To improve the radio-frequency performance, several circuit-level improvement techniques are proposed for the key building blocks in the front-end system. Furthermore, an advanced low-temperature co-fired ceramic process is developed to package the 39 GHz dual-channel transceiver chipset, and it achieves low packaging loss and high isolation between the two transmitting (TX)/receiving (RX) channels. Both the chip-level and system-in-package (SIP)-level measurements are conducted to demonstrate the performance of the transceiver chipset. The measurement characteristics show that the TX SIP provides 11 dB maximum gain and 10 dBm saturated output power, while the RX SIP achieves 52 dB maximum gain, 5.4 dB noise figure, and 7.2 dBm output 1 dB compression point. Single-channel communication link testing of the transceiver exhibits an error vector magnitude (EVM) of 3.72% and a spectral efficiency of 3.25 $bit \cdot s^{-1} \cdot Hz^{-1}$ for 64-quadrature amplitude modulation (QAM) modulation and an EVM of 3.76% and spectral efficiency of 3.90 $bit \cdot s^{-1} \cdot Hz^{-1}$ for 256-QAM modulation over a 1 m distance. Based on the chipset, a 39 GHz multi-beam prototype is also developed to perform the MIMO operation for 5G millimetre wave applications. The over-the-air communication link for one- and two-stream transmission indicates that the multi-beam prototype can cover a 5–150 m distance with comparable throughput.

1. Introduction

Fifth-generation (5G) wireless communication aims to provide high mobile data and low latency to meet various use cases, such as streaming video, augmented reality, playing three-dimensional (3D) games, automotive driving, and massive machine-type communication. Such requirements pose a key challenge for 5G front-end systems to feature large available bandwidths. According to the third Generation Partnership Project (3GPP) release, several spectra in millimetre wave (mmWave) bands have been issued for 5G new radio (NR), such as 28 and 39 GHz bands, which are extensions of the sub-6 GHz frequency range [1]. Due to the huge commercial market potential, 5G mmWave transceivers based on low-cost complementary metal-oxide semiconductor (CMOS) technologies have attracted tremendous attention from academic and industrial fields [2–7].

However, 5G mmWave communication systems suffer from higher free-space path loss and lower diffraction because of the smaller wavelengths [8,9]. Fortunately, the mmWave frequency facilitates high-gain antenna design by using an array with a large element number, which can compensate for the path loss to some extent. To meet the mobile demand, the 5G NR should also have beamforming and beam-scanning functionalities. To tackle the aforementioned technical challenges, some efforts have been made in the implementation of CMOS phased-array transceivers and related circuit techniques around 28 and 39 GHz in recent years [2–7,10–17]. Digital beamforming transceivers [5,16] and hybrid beamforming-based front-ends [6,7] feature high-performance beamforming and beam scanning; whereas, these systems are challenged by tremendous signal processing and hence require power- and area-hungry wideband digital processors. Refs. [3,11,12,18]

* Corresponding author.
E-mail address: kangkai@uestc.edu.cn (K. Kang).

https://doi.org/10.1016/j.eng.2022.04.023

introduce 28 GHz CMOS phased-array transceivers based on radio-frequency (RF) phase-shifting architectures as shown in Fig. 1(a), they achieve high integration. However, the phase/amplitude tuning in each RF channel will result in additional amplitude/phase variation, thereby deteriorating the performance of the entire system, particularly in their beamforming and beam-scanning accuracy. Additionally, over-the-air (OTA) testing and calibration for large-scale phased-array systems are time-consuming and expensive [19,20]. In Refs. [21,22], several built-in self-testing techniques are proposed to detect the amplitude and phase behaviors of mmWave phased-array transceivers, and they are able to effectively improve the testing efficiency and make rapid calibration possible. Ref. [10] reports a 39 GHz phased-array transceiver with built-in amplitude- and phase-calibration modules that alleviates the phase and amplitude mismatch of the transceiver channels. Nevertheless, these designs still suffer from certain detection/calibration deviations, complex circuit implementation, and large chip sizes.

To prominently increase the data rate and spectrum efficiency, many efforts have also been made in the architectures of the multi-stream beamforming front-ends. In addition to digital beamformers, the sub-array technique is popularly used for large-scale phased-array transceivers to achieve multi-beam operation [23,24]. The basic idea of the technique is to divide the antenna aperture of a phased array into several parts and form a certain number of beamformers; moreover, the number of beams and sub-array scale can be reconfigured to meet the different applications; however, this architecture requires complex control modules and sacrifices the gain of the antenna array. Dual-polarization phased-array transceivers have been also widely adopted in multi-beam systems; however, the beam number is usually limited to two [27,28]. Fully-connected phased-array front-ends are proposed in Refs. [6,25,26] which also feature multiple simultaneous beam formations, whereas the crossbar connection network is complicated and lossy and hence limits the overall array efficiency and scalability. In practice, phased-array-based mmWave systems also have disadvantages in terms of the time-consuming target searching and switching time between the base station (BS) and the user equipment (UE) which may be up to tens of milliseconds [29]. To alleviate these problems, several multi-stream systems are proposed based on photonic-aided beamformers [30,31], such as the Rotman lens; nevertheless, they are difficult to implement in UE equipment since they are bulky in size and their performance is sensitive to mechanical vibration and temperature variation [32]. Alternatively, a frequency-domain-multiplexing multi-input multi-output (MIMO) array with a single-wire interface is demonstrated in Ref. [33], while it requires multiple local-oscillator (LO) signals to simultaneously process different intermediate-frequency (IF) signals.

A dynamic multi-beam architecture and corresponding CMOS transceiver chipset are introduced to address these technical challenges. As presented in Fig. 1(b), the entire system incorporates a multi-beam antenna array, multi-beam selector, and transceiver chains. Since the beamforming relies on the antenna array and beam selector and every transceiver chain can manipulate an independent beam, the architecture does not need an additional phase and amplitude calibration process to realize accurate beam direction. Besides, the presented architecture is more flexible in controlling the beam number compared with phased-array systems. Each transmitting (TX)/receiving (RX) chipset consists of two TX/RX frequency-conversion channels. Several circuit techniques for key building blocks in the transceiver chipset are also introduced to obtain good linearity performance. To increase the output power and power efficiency, a gallium–arsenide (GaAs) power amplifier (PA) is added to each TX chain. As a result, the proposed MIMO architecture can achieve large coverage. The antenna array and beam selector are realized by substrate-integrated-waveguide (SIW) structures; thus, they have compact sizes and can be implemented on printed circuit boards (PCBs). From Table 1, it can be seen that although the proposed one has penalties of the system assembly complexity and flexibility of beam scanning, compared with the phased-array architectures, it has advantages in terms of the front-end chip implementation, beam control, speed of beam switch, and spectral efficiency.

For 5G mmWave applications, a high-performance package technology is also required. In this design, a low-temperature co-fired ceramic (LTCC) process, which presents low-loss dielectrics and reliable multilayer implementation [34], is developed for the mmWave transceiver chipset. Although the LTCC processes have been widely used in the mmWave passive circuit and component designs [35,36], the loss and thermal performances of LTCC-based packaging for mmWave large-scale chips must be further explored. In this article, we analyzed the high-frequency characteristics of the key structures in the LTCC package, including striplines, vertical via transition, and bonding wires.

This article expands upon our earlier work [37] and is organized as follows. Section 2 presents the system considerations and link budget analysis of the 39 GHz transceiver. Section 3 elaborates the circuit design of the transceiver. Section 4 introduces the LTCC-based package implementation. Section 5 illustrates the chip-level and system-in-package (SIP)-level measurement results and demonstrates the multi-beam prototype. Finally, this paper is concluded in Section 6.

2. Analysis and consideration of the system architecture

2.1. Link budget analysis

To facilitate circuit and system implementation, the link budget of the proposed 5G multi-beam architecture is analyzed. For the TX

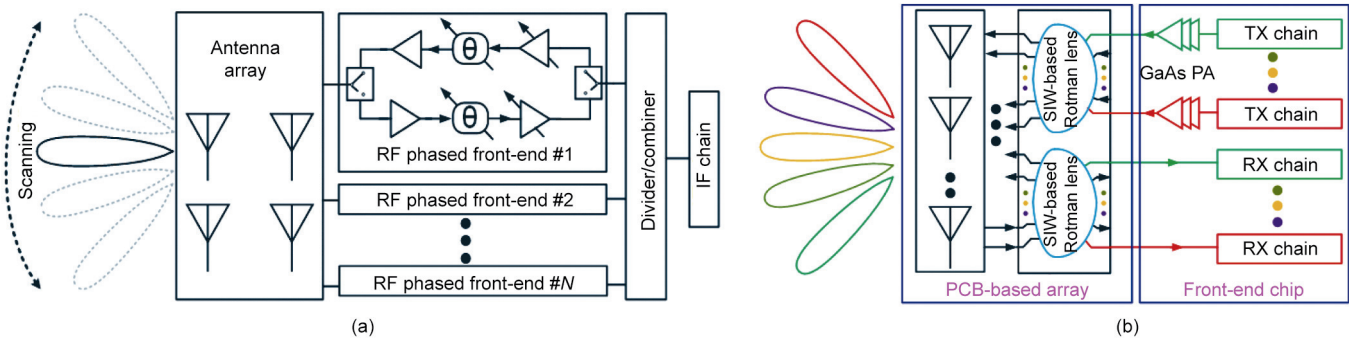


Fig. 1. System architectures for 5G NR. (a) Analog phase-shifting phased-array front-end; (b) proposed multi-beam MIMO front-end. IF: intermediate-frequency; PCB: printed circuit board; SIW: substrate-integrated-waveguide; TX: transmitting; RX: receiving; GaAs: gallium–arsenide; PA: power amplifier; *N*: number of the channel.

Table 1
Comparison of the phased-array and proposed dynamic multi-beam architectures.

Architecture	Features								
	Output power per channel	Flexibility of beam scanning	Complexity of beam control	Complexity of chip implementation	Assembly complexity	Phase calibration	Multiple beam	Speed of beam switch	Hardware cost
Phased-array architecture (Fig. 1(a))	Medium	High	High	High	Medium	Yes	No	Low	Low
Proposed dynamic multi-beam architecture (Fig. 1(b))	High	Medium	Low	Medium	High	No	Yes	High	Medium

mode, the targeting effective isotropic radiation power (EIRP) is set as 50 dBm for moderate/long-distance wireless communication, and it can be calculated by

$$\mathrm{EIRP} = P_t + G_{ANT} - L_{ANT} \quad (1)$$

where P_t, G_{ANT}, and L_{ANT} denote the output power of each TX channel, gain of the antenna array, and loss of the antenna's feed line, respectively. Since the SIW-based multi-beam antenna arrays that will be used have a G_{ANT} value of approximately 20 dBi and L_{ANT} value of 2 dB in the mmWave regime [38,39], P_t should reach 32 dBm to achieve the 50 dBm EIRP. However, this value is beyond the capability of a single PA in CMOS technology. Although the combination of multiple PAs can enlarge the output power, the power efficiency of the entire system will seriously deteriorate and the chip size will be too large [40]. To tackle these issues, a GaAs PA, as illustrated in Fig. 1(b), will be adopted in each TX channel. It has a gain of around 35 dB and an output 1 dB compression point (OP_{1dB}) of about 34 dBm. Because of the GaAs PAs, the CMOS chip only needs to deliver 0 dBm linear power. Note that the interconnection lines between the CMOS chip and GaAs PA may lead to considerable loss, which is estimated to be 3 dB. Therefore, the OP_{1dB} of the CMOS TX channel is set as 5 dBm to ensure a certain power margin.

For the RX mode, the RX signal power (P_r) can be learned by

$$P_r = \mathrm{EIRP} + 10 \times \lg\left(\frac{\lambda}{4\pi R}\right)^2 + G_{ANT} - L_{ANT} \quad (2)$$

where R and λ represent the working distance and the wavelength of the radiated electromagnetic (EM) wave in the air. $(\lambda/(4\pi R))^2$ is the path-loss factor. Based on Eq. (2), the theoretical P_r ranges from −30 to −45 dBm for a 50–300 m operating distance when the EIRP of the transmitter is 50 dBm. The input 1 dB compression point (IP_{1dB}) per channel is thus chosen as −25 dBm to maintain a reasonable dynamic range and tolerate interference from other BSs. Based on the 3GPP release, the 39 GHz transceiver is required to support a 400 MHz signal bandwidth. To perform the 64-quadrature amplitude modulation (QAM) modulation, the error vector magnitude (EVM) should be lower than 8%, and the minimum corresponding signal-to-noise ratio (SNR_{min}) of the RX channel is 22 dB. For a targeting receiver sensitivity of −58 dBm, the noise figure (NF) of the RX link can be derived based on the given signal bandwidth and SNR_{min} [41], which needs to be less than 8 dB. Considering an L_{ANT} of 2 dB, the NF of the CMOS chip should be smaller than 6 dB. Since analog-to-digital converters in the baseband circuits need 7 dBm driving power, the gain of the CMOS RX channel is set as more than 47 dB. To meet the requirements of different application scenarios, the CMOS chip should also integrate gain-controlling blocks to control the output power of the transmitter and extend the dynamic range of the receiver. In this work, the gain-tuning range of each channel is set as 31 dB with a 1 dB gain-tuning step. Through the literature review and EM simulation, the mutual coupling among different beam ports of the used SIW-based beam selector is learned, which is less than −20 dB in the mmWave range. Therefore, the isolation between the two channels in the CMOS chip is set to be larger than 30 dB to avoid worsening the crosstalk of the entire system. The key system specifications of the CMOS chip are summarized and listed in Table 2.

2.2. CMOS transceiver architecture

Besides the aforementioned requirements, several significant preconditions for CMOS chips should be addressed: ① high scalability for multi-beam MIMO applications; ② low complexity of interconnection between the CMOS chips and other modules in system boards; ③ proper input/output (I/O) interface design to minimize the performance degradation caused by system routing; ④ symmetrical layout and high channel isolation to ensure channel consistency; and ⑤ compact packaging for mmWave CMOS chips to mitigate the assembly difficulty and cost of large-scale MIMO systems.

To tackle the above technical challenges, an architecture for the CMOS chipset is proposed and shown in Fig. 2. Both the TX and RX chips consist of two channels, an LO chain, and a serial peripheral interface (SPI) module. Each TX channel is comprised of an IF mixer, RF mixer, five-bit attenuator, and PA; while the RX channel consists of a low noise amplifier (LNA), five-bit attenuator, RF mixer, IF mixer, and IF amplifier. To minimize LO leakage and improve image rejection, a superheterodyne topology is adopted in this work. As illustrated in Fig. 2, the frequency schemes of RF, internal IF, and external IF are set to 38.5, 11.5, and 2.5 GHz, respectively. The corresponding LO frequencies of the RF and IF mixers are 27 and 9 GHz, respectively. A 9 GHz

Table 2
Key specifications of the CMOS chip for the 5G multi-beam MIMO system.

Parameter	Value
RF	38.5 GHz
LO frequency	9 GHz
IF	2.5 GHz
Number of TX/RX channel	2
Support modulation	64-QAM
Required SNR	22 dB
OP_{1dB} of TX	5 dBm[a]
IP_{1dB} of RX	−25 dBm
NF	6 dB
Gain tuning range/step of TX/RX	31 dB/1 dB
Channel isolation of CMOS chip	> 30 dB

SNR: signal-to-noise ratio.
[a] Including 2 dB link margin.

sinewave signal from an off-chip module is injected into the chip to provide the LO signal for the IF mixer. Because the LO frequency of the RF mixer ($f_{RF\text{-}LO}$) is three times that of the IF mixer ($f_{IF\text{-}LO}$), a injection-locked frequency tripler (ILFT) is employed to multiply the externally input LO signal and generate the RF mixer's LO. Compared with the conventional architecture with an on-chip phase-locked loop (PLL) [42], the LO chain exploits the benefits of the simple circuit design and compact layout. Furthermore, based on the LO chain, the chipset is easy to assemble a larger MIMO system.

In practice, mmWave multi-channel transceivers based on CMOS technologies suffer from some disadvantages in terms of poor substrate isolation and layout-dependent parasitics. Therefore, fully differential structures are used to implement all the building blocks in the transceiver, which are robust to the severe parasitic effects of ground and supply lines as well as those of packages. Three baluns are employed in the RF and LO chains to convert the single-ended/differential signal into the differential/single-ended form.

3. Circuit implementation

3.1. Transmitter channel

As presented in Fig. 2(a), the TX channel adopts the superheterodyne architecture. To attain high linearity and LO isolation to deal with the large input IF signal and LO self-mixing, a double-balanced Gilbert topology with a linearity-enhancement technique is employed to design both the IF and RF up-conversion mixers. As shown in Fig. 3(a), the transconductance (g_m) stage is composed of a common-source (CS) structure with source-degeneration inductors and a common-gate (CG) structure. The CS transistors M_{R1} and M_{R4} are biased in the saturation region, while the CG transistors M_{R2} and M_{R3} work in the weak inversion region. Under this bias condition, the third-order g_m of the CS transistors has the opposite polarity to that of the CG transistors. By optimizing the bias voltages and device sizes of the CS and CG structures, the summed third-order g_m of the two paths can be eliminated, which improves the linearity of the circuits [43].

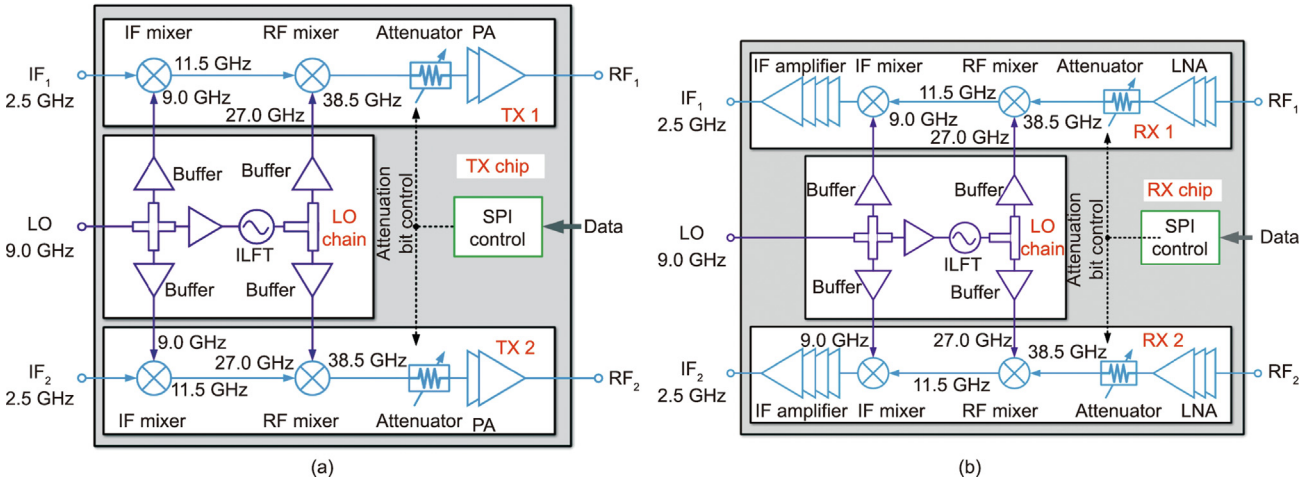


Fig. 2. Diagrams of the proposed TX and RX chips. (a) TX; (b) RX. ILFT: injection-locked frequency tripler; SPI: serial peripheral interface; LNA: low noise amplifier.

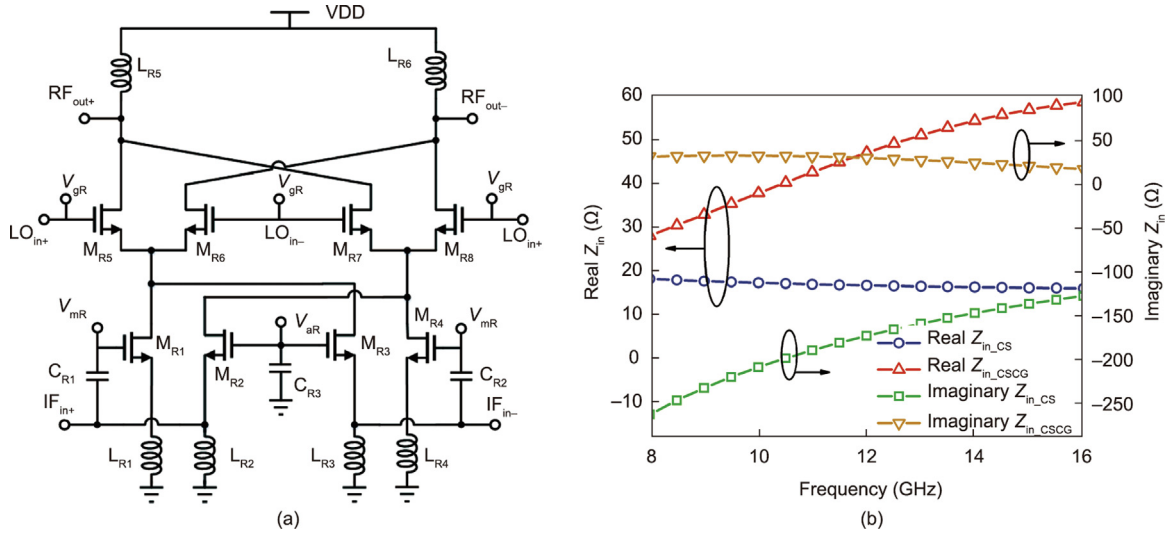


Fig. 3. (a) Schematic of the RF and IF up-conversion mixers; (b) simulated input impedance of the CS stage and CSCG stage. M_{R1}–M_{R8}: transistors in the schematic; L_{R1}–L_{R6}: inductors in the schematic; C_{R1}–C_{R3}: capacitors in the schematic; VDD: supply voltage; V_{mR}: bias voltage of the transistors M_{R1} and M_{R4}; V_{aR}: bias voltage of the transistors M_{R2} and M_{R3}; V_{gR}: bias voltage of the transistors M_{R5}–M_{R8}; IF_{in+}, IF_{in-}: input IF signal; LO_{in+}, LO_{in-}: input LO signal; RF_{out+}, RF_{out-}: output RF signal; Z_{in}: the input impedance; Z_{in_CS}: the input impedance of the conventional Gilbert mixers; Z_{in_CSCG}: the input impedance of the proposed topology.

Due to the parasitic gate-to-source capacitor of M_{R1}, the input impedance of the conventional Gilbert mixers (Z_{in_CS}) encounters a large imaginary part and a sharp variation along with the operating frequency as illustrated in Fig. 3(b). This limits the input matching bandwidth. Extra components, such as large inductors, are required to deal with the large imaginary part of the input impedance, which will lead to some penalty of the chip area and loss. However, the input impedance of the proposed topology (Z_{in_CSCG}) is determined by both the CS and CG paths' input impedances. The simulated Z_{in_CSCG} is also plotted in Fig. 3(b), whose imaginary part is much smaller and has flatter frequency response than that of Z_{in_CS}. This finding indicates that the proposed topology can easily achieve wideband impedance matching with a previous stage or source impedance (50 Ω). The post-layout simulation shows that the up-conversion mixers achieve a gain of around 0 dB and −1 dBm IP_{1dB} at 38.5 GHz while consuming 34.2 mW direct-current (DC) power.

The RF up-conversion mixer is followed by a five-bit attenuator as shown in Fig. 4(a). The 1, 2, and 4 dB attenuation cells are realized by a bridge-T topology, while the 8 and 16 dB attenuation cells adopt a π-type topology. To reduce the phase variation during different states, a tail capacitor C_{t1}/C_{t2} is introduced in the shunt branch of each attenuation cell [44]. From Fig. 4(b), it can be observed that the phase response of the attenuation cell is sensitive to C_{t1}/C_{t2}. Therefore, the phase delay in the attenuation state will be compensated by C_{t1}/C_{t2}; hence, the phase difference between the attenuation and reference states can be effectively minimized. In this design, C_{t1}/C_{t2}s of the 1, 2, 4, 8, and 16 dB attenuation cells are 71, 27, 46, 30, and 34 fF, respectively. As illustrated in Fig. 4(b), the measured root-mean-square (RMS) phase error of the attenuator is lower than 3.8° across 37–41 GHz. In addition, a large resistor is added to the bulk nodes of the switches M_{A1-A4} to prevent RF signal leakage from transistors' channels to the ground, thereby decreasing the loss. As a result, the attenuator achieves an amplitude range of 31 dB with 7 dB loss.

As presented in Fig. 5, the PA is realized by a two-stage differential three-stacked structure. The transistors are biased in class-AB mode to balance the linearity and power efficiency. By stacking three transistors, the supply voltage can be prominently improved without operating transistors beyond the breakdown voltage. The output power is also enhanced accordingly. Compact 1:1 transformers (TF_{P1} and BN_{P1}) are employed to serve as the input and output matching networks. BN_{P1} also transfers the differential signal to the single-ended mode for the measurement and package requirements. In this design, the supply voltage for the PA is set as 1.8 V. It draws a 50 mA DC current and delivers a linear output power of 7.5 dBm at 38.5 GHz according to the post-layout simulation.

3.2. Receiver channel

Similar to the TX channel, the RX channel also adopts a dual-conversion architecture and is composed of an LNA, a five-bit attenuator, two down-conversion mixers, and an IF high-gain amplifier. The attenuator is same as that in the TX channel. To compensate for the attenuator's loss and suppress the following

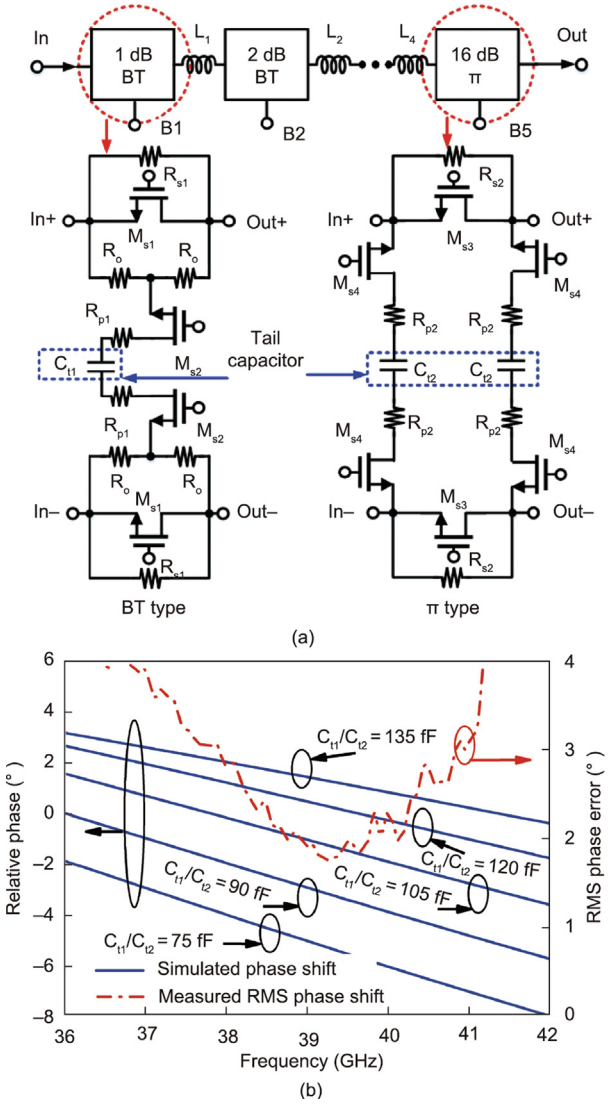


Fig. 4. (a) Schematic of the attenuator; (b) simulated phase response of the 8 dB attenuation cell and measured RMS phase error of the attenuator. RMS: root-mean-square; BT: bridge-T; L_1, L_2, L_4: series inductors for the inter-stage impedance matching; B_1, B_2, B_5: logical controlling bits; R_{s1}, R_{s2}: the resistors in the series branches of the circuit; M_{s1}–M_{s4}: transistors in the circuit; R_o, R_{p1}, R_{p2}: the resistors in the parallel branches of the circuit; C_{t1}, C_{t2}: tail capacitors.

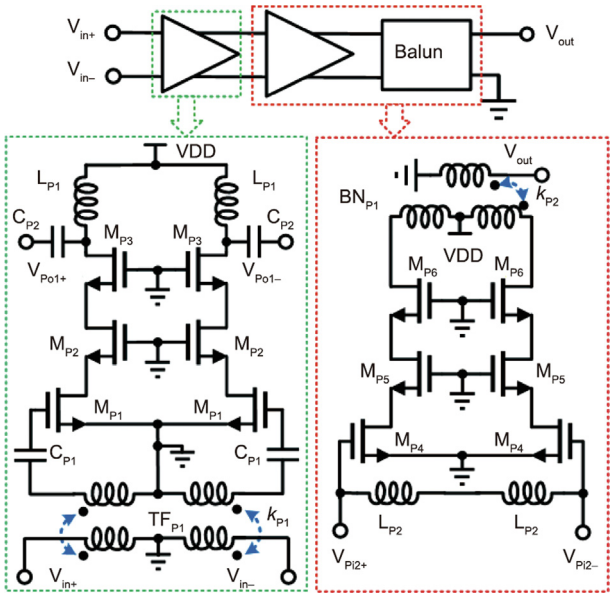


Fig. 5. Schematic of the PA. V_{in+}, V_{in-}: input differential signal; V_{out}: output single-ended signal; V_{Po1+},V_{Po1-}: output signal of the first stage; V_{Pi2+}, V_{Pi2-}: input signal of the second stage; TF_{P1}: input transformer of the PA; k_{P1}: coupling coefficient of TF_{P1}; L_{P1}: load inductors of the first stage; L_{P2}: input-matching inductors of the second stage; C_{P1}, C_{P2}: capacitors in the PA; M_{P1}–M_{P6}: transistors in the PA; BN_{P1}: output balun of the PA; k_{P2}: coupling coefficient of BN_{P1}.

stages' noise contribution, a three-stage topology is used to implement a high-gain LNA, as shown in Fig. 6(a). The first stage is realized by a CG topology with a transformer-based g_m-boosting technique to achieve both the input impedance matching and noise matching, thus improving both the gain and noise performance. The second and third stages are based on a CS structure. Cross-coupled capacitors are used in the last two stages to neutralize parasitic gate-to-drain capacitors to obtain high gain. A transformer-based positive feedback network between the source and drain nodes of the transistors M_{L2} is also employed to further reduce the noise contribution of the second stage and extend the inter-stage matching bandwidth [45]. The stability performance is another critical challenge for the proposed LNA because it has a gain of more than 30 dB. Thanks to the capacitive neutralization technique and the feedback transformer in the second stage, the LNA has good stability in the differential mode. However, the undesired common-mode signal, which is caused by the imbalance of the balun and mismatch of the devices and interconnects, will be amplified by each stage of the LNA, which may lead to a risk of oscillating. As shown in Fig. 6(b), the simulated common-mode stability factor of the traditional structure is less than 1 across 31.5–34.6 GHz. To solve the problem, a transmission line (TL) is added to the common-mode point of the third stage to suppress the common-mode signal. As a result, the LNA achieves excellent stability in both the differential and common modes due to these methods (Fig. 6(b)). According to the circuit simulation, the LNA, which draws 48 mW DC power, attains a gain of 30.5 dB, NF of 3.9, and IP_{1dB} of −23 dBm at 38.5 GHz.

Fig. 7(a) shows the topology of the IF and RF down-conversion mixers. The g_m stage uses a CG structure for wideband impedance

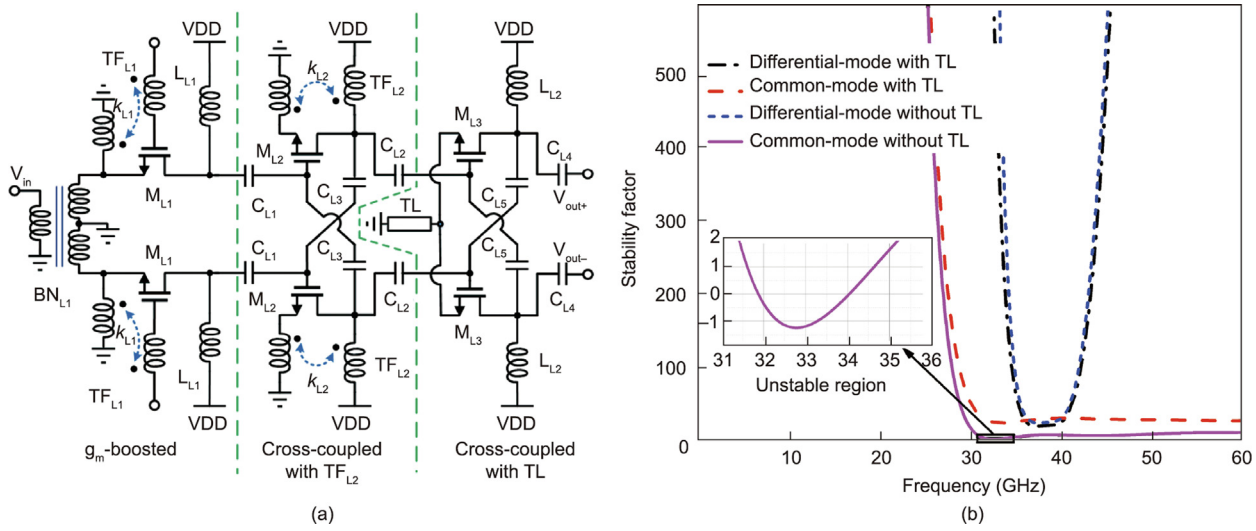


Fig. 6. (a) Schematic of the LNA; (b) post-layout simulated differential-mode and common-mode stability factors.V_{out+}, V_{out-}: output differential signal; V_{in}: input single-ended signal; TL: transmission line; BN_1: input balun; TF_{L1}: transformer in the first stage of the LNA; k_{L1}: coupling coefficient of TF_{L1}; TF_{L2}: transformer in the second stage of the LNA; k_{L2}: coupling coefficient of TF_{L2}; L_{L1}, L_{L2}: inductors in the schematic for impedance matching; M_{L1}–M_{L3}: transistors in the schematic of the LNA; C_{L1}–C_{L5}: capacitors in the schematic of the LNA.

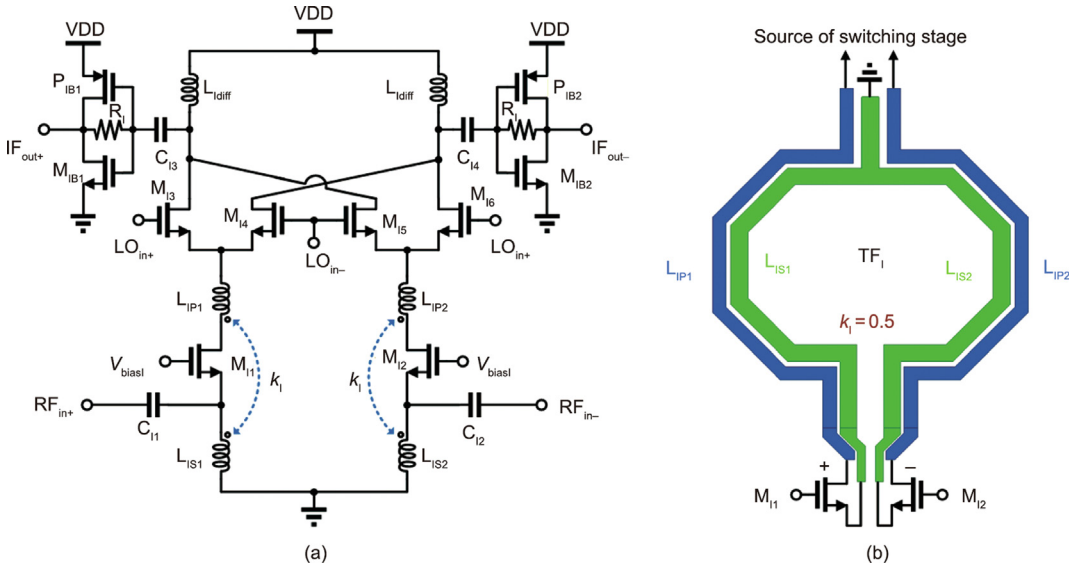


Fig. 7. (a) Schematic of the RF and IF down-conversion mixers; (b) implementation of the transformer feedback. V_{biasI}: gate bias voltage of the transconductance stage; RF_{in+}, RF_{in-}: input RF signal; IF_{out+}, IF_{out-}: output IF signal; P_{IB1}, P_{IB2}: positive-channel transistors in the output buffer of the mixer; M_{IB1}, M_{IB2}: negative-channel transistors in the output buffer of the mixer; R_I: feedback resistors in the output buffer of the mixer; C_{I1}–C_{I4}: capacitors in the schematic; M_{I1}–M_{I6}: transistors in the mixer; L_{Idiff}: differential load inductors in the mixer; L_{IP1}, L_{IP2}: drain inductors of the transconductance stage; L_{IS1}, L_{IS2}: source inductors of the transconductance stage; TF_I: transformer in the mixer; k_I: coupling coefficient of TF_I.

matching. To enlarge the gain, a transformer-based feedback technique is used between the source and drain nodes of the g_m stage transistors M_{I1} and M_{I2}. Fig. 7(b) depicts the physical structure of the differential transformer. In addition, the transformer reduces the coupling between the g_m and switching stages, thus enhancing the LO-to-RF isolation. The RF down-conversion mixer consumes 10.5 mA current under 1.8 V supply voltage and achieves 7.3 dB gain and −5.9 dBm IP_{1dB} at 38.5 GHz.

As illustrated in Fig. 2(b), the IF mixer is followed by a four-stage IF amplifier. Fig. 8 shows the schematic of the circuit. The first three stages are realized by a CG structure with a current-source load. To suppress the common-mode signal, a resistor R_{I1} is inserted between the common-mode path and ground in the first two stages. The final power stage uses the cascode structure with an inductive differential load to deliver high output power (Fig. 8). With a 1 V supply voltage, the cascode amplifier can also undergo a high voltage swing at the drain node. To conserve the chip size, the inductorless method is used to tandemly connect the amplification stages. The measurement results show that the IF amplifier has a 27 dB gain and 8 dBm OP_{1dB} at 2.5 GHz with a power consumption of 37.4 mW.

3.3. LO chain

The LO chain, as presented in Fig. 2, is used to provide the LO signals for both the IF and RF mixers in the two TX/RX channels. An external 9 GHz LO signal is input and transferred into the differential form by an on-chip balun. The balun is realized by using a 3:3 transformer with a coupling coefficient of 0.72 (Fig. 9(a)). Both the primary and secondary windings use the top metal to attain a high quality factor. The EM simulated phase error, amplitude mismatch, and loss are 0.5°, 0.25 dB, and 2.5 dB at 9 GHz, respectively. Then, the differential input signal is split into three parallel paths by a differential power divider to drive the two IF mixers and an ILFT. In addition, three identical IF buffers are added to the three parallel paths to compensate for the loss triggered by the balun and power divider, and they also provide a constant load impedance for the three paths of the power divider, thus minimizing the imbalance of LO power for the different channels. With the ILFT, the external input LO signal's frequency is multiplied by three. The generated third-order harmonic signal is divided into two paths by a compact passive divider and amplified by two parallel RF buffers to drive the two RF mixers in the TX/RX chip. To save the chip area, the power divider is reused as the inter-stage matching networks, and their layouts are designed to be as symmetrical as possible to minimize inconsistencies in the LO input power to the two channels, as shown in Fig. 9(b). All the buffers in the LO chain are realized by a CS topology with a differential inductive load to obtain adequate gain and output power, as presented in Fig. 9(c).

Fig. 9(d) illustrates the schematic of the ILFT. For the injection-locked oscillator, the locking range is dominated by the amplitude of the third-order harmonic injected into the oscillator [46]. Therefore, the transistors M_{T5} and M_{T6} for harmonic generation are designed with a conduction angle of 100° for the maximum third harmonic component. Besides, the feedback resistors R_{T1} and R_{T2} are employed to further improve the locking range. The varactors C_{T1} and C_{T2} are adopted to compensate for the process, voltage, and temperature (PVT) variations. The measured locking range of the ILFT is from 8.40 to 9.66 GHz with an input power of 0 dBm and 4.6 mW DC power consumption. Fig. 9(e) shows the measured phase-noise performance. The phase noise of the output signal of 27 GHz at an offset of 1 MHz is −125.1 dBc, while that of the input signal of 9 GHz is −134.9 dBc. The phase-noise degradation is 9.8 dB, which is close to the theoretical value of 9.5 for frequency multipliers with a multiplication ratio of 3. Therefore, the ILFT has a small impact on the phase-noise performance of the LO signal for the transceiver.

3.4. Layout consideration

Thanks to the differential structures, the layouts of the mmWave circuits are designed symmetrically to minimize the effects of the parasitics of the ground and supply lines and hence maintain good RF performance. To minimize the layout-dependent effects and ensure good consistency of the channel response, layouts of the two TX/RX channels are also placed as symmetrically as possible. The LO chain and SPI module are inserted between the two TX/RX channels, which leads to equal-length and symmetrical LO feeding structures for each channel (Fig. 9(b)). Due to the symmetrical layout, the LO chain provides equal driving power to the mixers in the two channels. It also guarantees considerably high channel isolation. In addition, metallic barriers that are stacked from the substrate to the top metal and connected to the ground plane, are utilized in each channel to further improve the channel isolation.

4. LTCC-based packaging design

Compared with conventional packaging processes, the LTCC package features higher reliability and relatively lower loss in

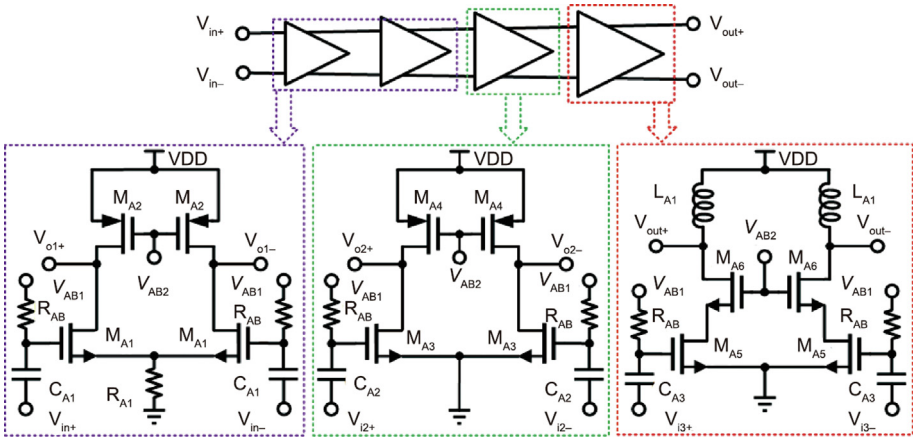


Fig. 8. IF amplifier's schematic. M_{A1}–M_{A6}: transistors in the IF amplifier; R_{AB}: bias resistors; R_{A1}: source-degeneration resistor in the first/second stage; C_{A1}–C_{A3}: capacitors in the circuit; L_{A1}: load inductors of the IF amplifier; $V_{i2/3+}$, $V_{i2/3-}$: input signal of the third/fourth stage of the IF amplifier; $V_{o1/2+}$, $V_{o1/2-}$: output signal of the first/third stage of the IF amplifier; V_{AB1}: gate bias voltages of the common-source transistors; V_{AB2}: gate bias voltages of the common-gate transistors.

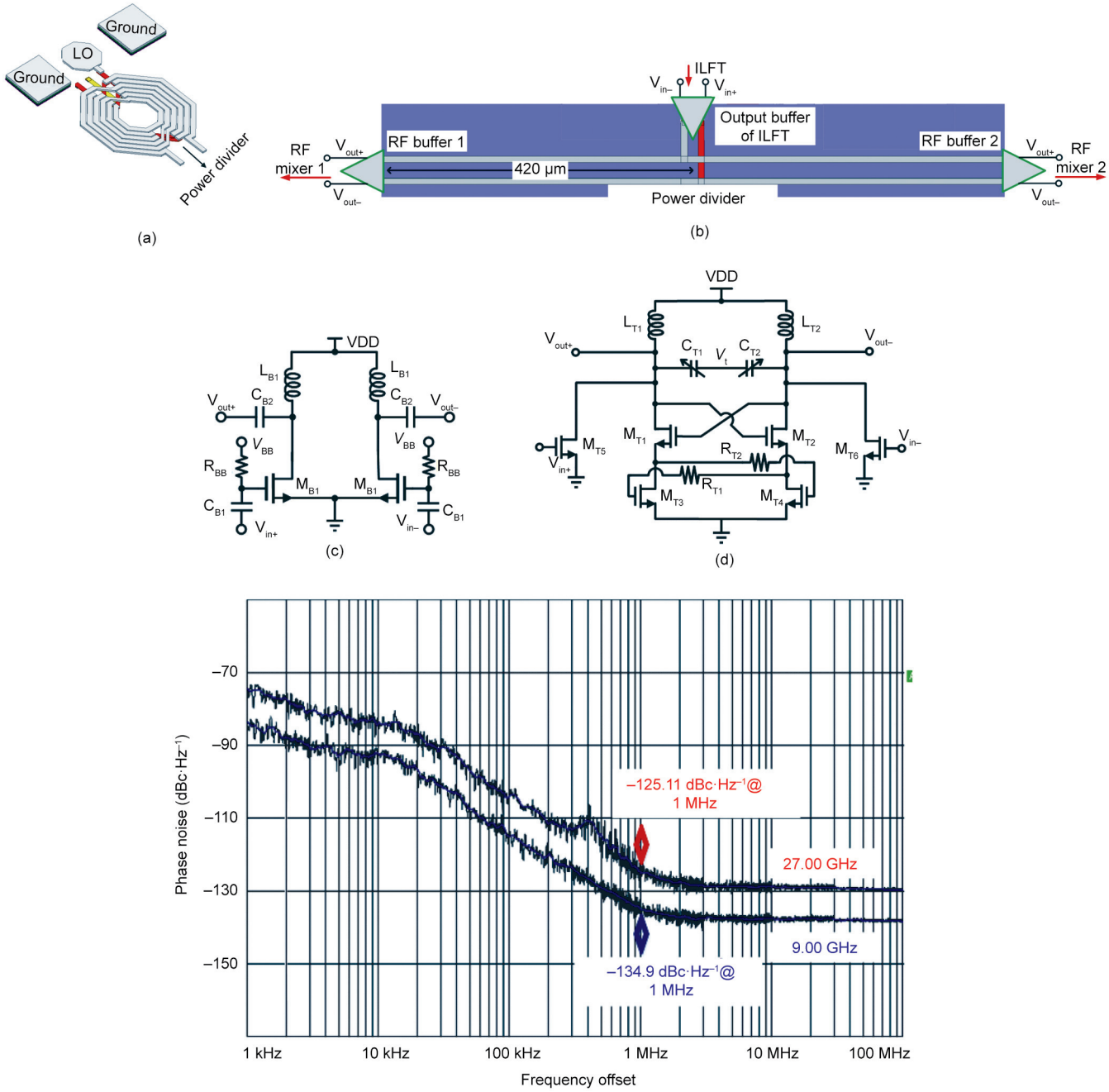


Fig. 9. (a) 3D view of the LO input balun; (b) layout view of the RF passive divider with the buffers; (c) buffers' topology; (d) schematic of the ILFT; (e) measured phase noise of the ILFT. V_{BB}: gate bias voltage of the buffer; L_{B1}: load inductors of the buffer; R_{BB}: bias resistors of the buffer; M_{B1}: transistors in the buffer; C_{B1}, C_{B2}: capacitors in the buffer; M_{T1}–M_{T6}: transistors in the ILFT; L_{T1}, L_{T2}: drain inductors in the ILFT; C_{T1}, C_{T2}: varactors in the ILFT; R_{T1}, R_{T2}: gate resistors in the ILFT; V_t: tuning voltage of the varactors.

mmWave bands. Therefore, it is adopted to package the 39 GHz transceiver chipset. Figs. 10(a) and (b) show the 3D and top views of the LTCC packaging. It consists of 18 layers of insulator substrate (Ferro A6 with a thickness of 92 μm and relative dielectric constant (ε_r) of 6.0) and 19 metal layers (silver with a thickness of 8 μm). Four ground planes (first layer, eighth layer, twelfth layer, and nineteenth layer) separate the package box into three functional regions: digital control (layers 2–7), RF signal stripline (layers 9–11), and power supply (layer 13–18). These regions minimize the crosstalk among the different types of signals. The package size is approximately 9.000 mm × 9.000 mm × 1.826 mm.

A 3 mm × 3 mm cavity with a depth of 300 μm is excavated to place the chip; thus, the CMOS chip and top layer of the package have the same height. The structure shortens the length of the bonding wires from the chips to the package and mitigates the severe impact of bonding wires in the mmWave regime. The TX and RX chips are designed with similar layout frameworks. Therefore, they share the same package structure. Since the RF port locations of the TX chip are distinct from those of the RX chip, two extra RF signal striplines are added in the package, as shown in Fig. 10(b). This shared package can simplify the system assembly and decrease the packaging cost.

4.1. Signal stripline and vertical via transition design

Fig. 11(a) shows the RF signal transmission structure. It is comprised of a coplanar waveguide (CPW) bonding finger, vertical via transition I, RF stripline, vertical via transition II, and CPW surface

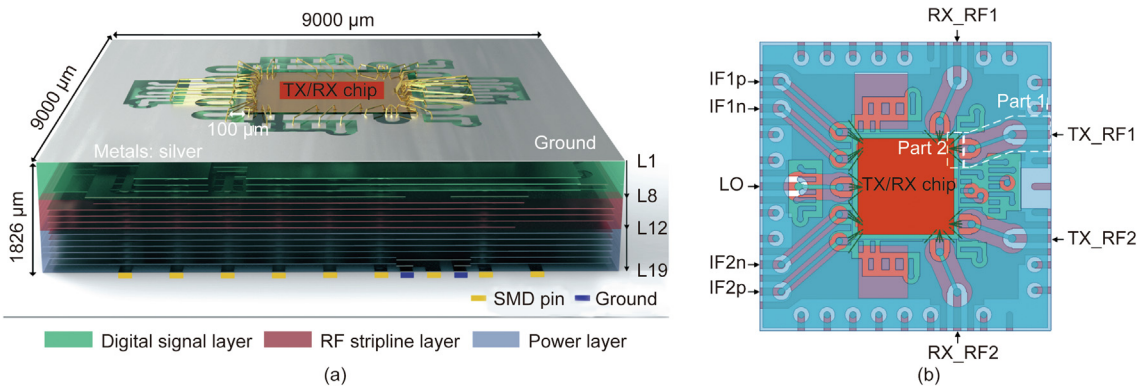


Fig. 10. Physical structure of the LTCC package. (a) 3D view; (b) simplified top view (only shows the signal paths). SMD: surface mounted device; IF1p, IF1n: the first IF I/O ports; IF2p, IF2n: the second IF I/O ports; RX_RF1/RX_RF2: RF input port of the first/second RX channel; TX_RF1/TX_RF2: RF output port of the first/second TX channel; L1: the first layer; L8: the eighth layer; L12: the twelfth layer; L19: the nineteenth layer.

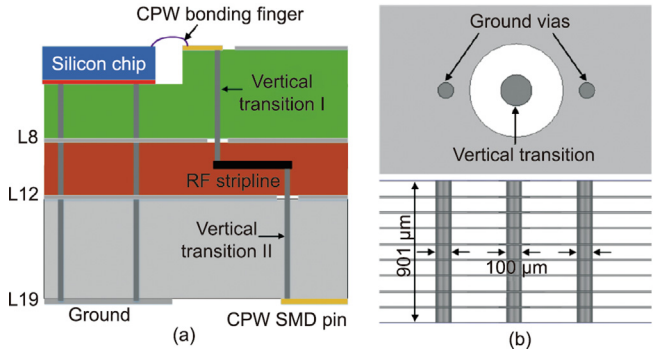


Fig. 11. (a) Cross-sectional view of the RF signal transmission path; (b) vertical via transition. CPW: coplanar waveguide.

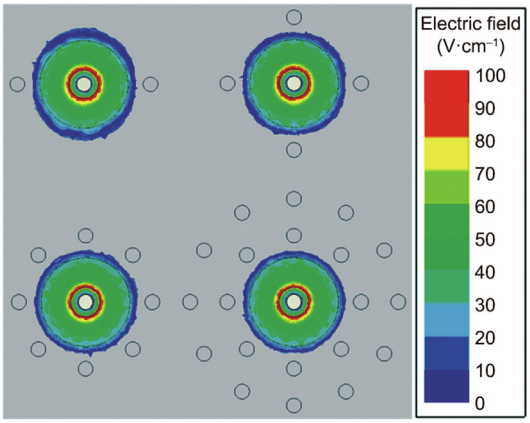


Fig. 12. Electric-field distribution versus the number (2, 4, 8, 20) of ground vias.

Fig. 13. Coupling model between two vertical via transitions of adjacent channels.

mounted device (SMD) pin. The stripline is implemented on the tenth layer, while the ground planes are implemented on the eighth and twelfth layers. The upper and lower symmetrical ground surfaces lead to uniform electric field distribution and provide an effective EM shield [47]. In addition, two rows of ground vias on both sides of each stripline are used to further reduce the EM dispersion and radiation. Therefore, the loss of the stripline will be reduced, and the interference from other striplines can be isolated.

Two rows of ground vias are also employed around the vertical via transitions which are used for interconnections between the CPW line and stripline. To investigate their characteristics, an EM simulation is conducted for the vertical via transition I. As depicted in Fig. 11(b), the height and diameter of the vertical vias are 901 and 100 μm, respectively. Fig. 12 presents the top view of the simulated electric-field distributions around the vertical via transition with different numbers of ground vias. It can be seen that the electric field is constrained more strictly inside the vias along with the increase in the number of ground vias. The EM simulation result shows that the losses of transition with 2, 4, 8, and 20 ground vias are around 0.200, 0.120, 0.100, and 0.095 dB at 39 GHz, respectively. The EM coupling effect among adjacent channels' transitions, which is shown in Fig. 13, is also studied. The simulated EM coupling between Port 1 and Port 4 is −64.0 dB with a circle of ground vias, while that is −85.7 dB with two circles of ground vias. Therefore, the ground vias not only can reduce the loss but also mitigate the crosstalk among the adjacent channels. In this design, two circles with a total of 20 ground vias are adopted to implement the vertical via transition to balance the RF performance and package size.

4.2. Bonding-wire transition

The bonding-wire transition is another pivotal component in the mmWave package. Although the cavity is used to shorten the lengths of bonding wires, the wires still have a considerable impact on the entire performance of the system, particularly those at RF terminals. Fig. 14(a) shows the 3D view of a bonding-wire transition between the ground-signal-ground (GSG) pads and CPW bonding finger. Fig. 14(b) depicts the physical structure of the golden bonding wires, which have a diameter, length, and height of 25, 250, and 100 μm, respectively. To ensure the simulation accuracy, the packaging model for EM simulation includes all the bonding wires and signal transmission structures. Fig. 15 displays the EM simulated reflection coefficients of the port looking into the SMD pin and the losses with different numbers of bonding wires at an RF terminal. The trough of the reflection coefficient moves to a higher frequency, and the loss decreases when the number of the bonding wires increases. Because the equivalent inductance and parasitic resistance will proportionally decrease

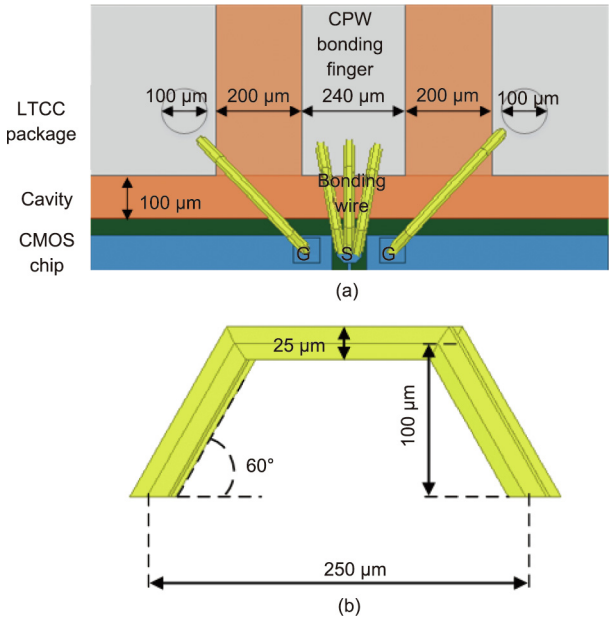


Fig. 14. (a) Bonding-wire transition between the GSG pads and CPW bonding finger; (b) physical structure of the golden bonding wire. GSG: ground-signal-ground.

as the parallel bonding wires increase. However, the size of the pad limits the number of accommodatable bonding wires. In this design, we used three bonding wires at each RF pad to maintain good RF performance and impedance matching, while the DC and ground pads only use one bonding wire to reduce costs.

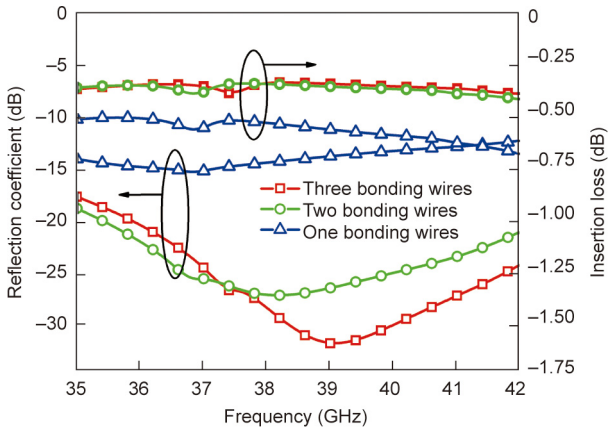


Fig. 15. Simulated reflection coefficient and loss with the different numbers of the bonding wires.

5. System measurements and discussion

The 39 GHz two-channel transceiver chipset is fabricated in a standard 65 nm CMOS process and mounted in the LTCC package. The die photos and testing boards are shown in Fig. 16. The TX chip size is 2.4 mm × 2.8 mm, while the area of the RX chip is 2.8 mm × 2.8 mm. The TX and RX chips share the same LTCC package which is approximately 9 mm × 9 mm. The transceiver chipset

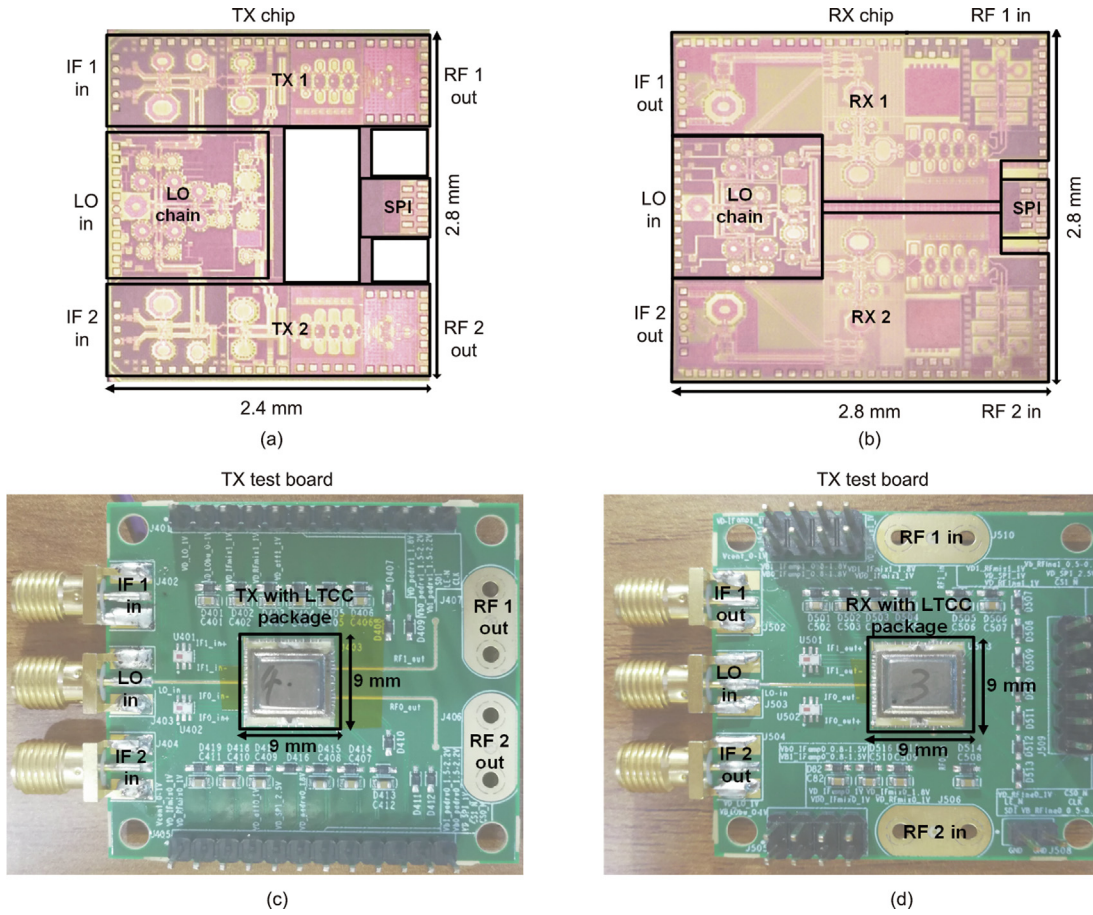


Fig. 16. (a) Die photo of the TX chip; (b) die photo of the RX chip; (c) test board of the TX front-end system in the LTCC package; (d) test board of the RX front-end system in the LTCC package. Reproduced from Ref. [37] with permission.

is subjected to chip-level measurement and SIP-level measurement. Based on the designed chipset, a 39 GHz multi-beam MIMO prototype is developed for 5G NR. The OTA testing of the TX-to-RX communication link is also conducted to demonstrate the functionality of the 5G NR systems.

5.1. Chip-level and SIP-level measurements

The chip-level and SIP-level measurement setups are shown in Figs. 17(a) and (b), respectively. The chip-level measurement for the gain and linearity performances is performed by a vector network analyzer (VNA). All DC, SPI I/O, IF, and LO pads are connected to PCB traces by golden bonding wires. An off-chip IF balun is used to convert the differential IF signal into the single-ended mode for measurement. An automatic testing system is also developed to capture the SIP-level performance.

Fig. 18 shows the simulated and measured RF-port impedance-matching characteristics of the TX and RX chips. The reflection coefficient at RF ports of the RX chip is lower than −10 dB across 36.3–42.0 GHz, while that of the TX chip is about −6 dB in the targeting band. The reason for the relatively poor impedance matching of the TX chip is that the reflection coefficient of the PA is sacrificed to improve the output power and power efficiency. Due to the relatively poor output matching, an interaction occurs between the CMOS TX chip and GaAs PA, and the gain and output power of the TX system deteriorate to some extent. However, the CMOS TX's OP_{1dB} has a nearly 2 dBm margin, and we can adjust the attenuator and input signal power to compensate for the loss. The SIP-level simulation and measurement are also presented in Fig. 18, and they take PCB transmission lines and 2.92 mm connectors into account. It can be observed that the SIP-level measured reflection coefficients agree well with the chip-level reflection coefficients, which indicates that the package-related degradation of the RF performance is significantly mitigated.

The measured conversion gains of the TX and RX channels with the LTCC package are presented in Figs. 19(a) and (b), and they are approximately 52.2 and 11.3 dB at 38.5 GHz, respectively. The losses of the IF balun and connectors are de-embedded in the testing. From Fig. 19, it can also be seen that the achieved RF bandwidths of the TX/RX chips are larger than 2 GHz. For multi-channel on-chip systems, channel isolation is another critical specification. Therefore, the channel isolations of the TX and RX front-end systems in the package are measured and presented in Fig. 19. Benefiting from the fully symmetrical layouts of the chips and package used, the RX system's channel isolation is better than 51 dB across 37–40 GHz, while that of the TX system is higher than 60 dB. The 32 measured gain stages of the TX SIP and RX SIP versus IF frequency are plotted in Figs. 20(a) and (b). The measured gain variation range is about 33 dB, which is slightly larger than the expected value of 31 dB. The main reason is that the attenuation cells are sensitive to the impedance of the adjacent cells and stages, especially the 8 and 16 dB attenuation cells. Besides, the deviation

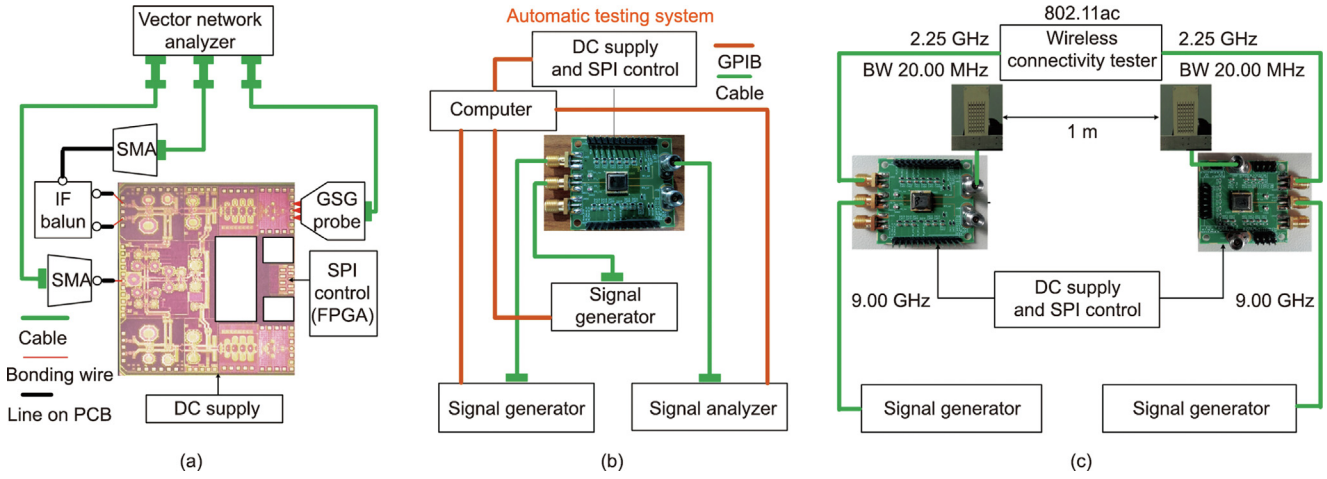


Fig. 17. Measurement setups. (a) On-chip testing; (b) SIP-level testing; (c) testing of the single-channel TX-to-RX wireless link. FPGA: field-programmable gate array; SMA: small A type; GPIB: general-purpose interface bus; BW: bandwidth.

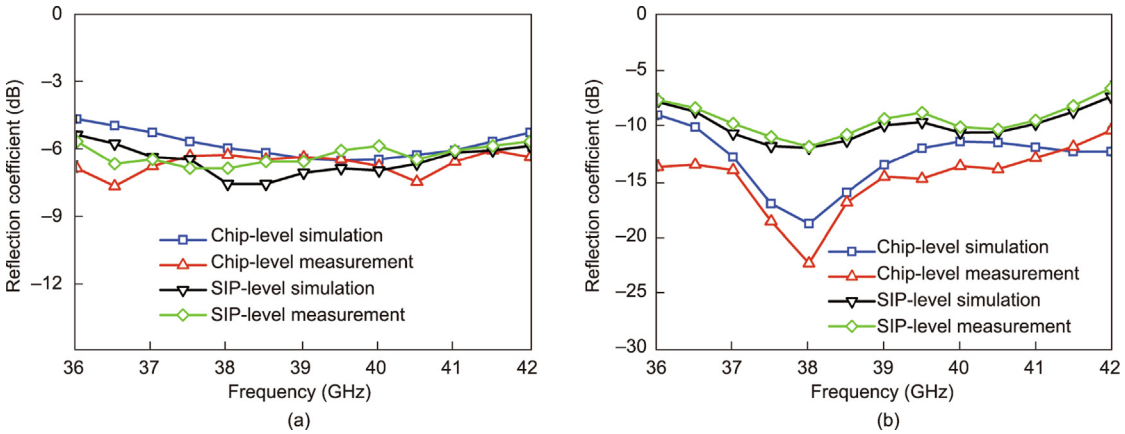


Fig. 18. Measured and simulated reflection coefficients with and without the package. (a) TX; (b) RX.

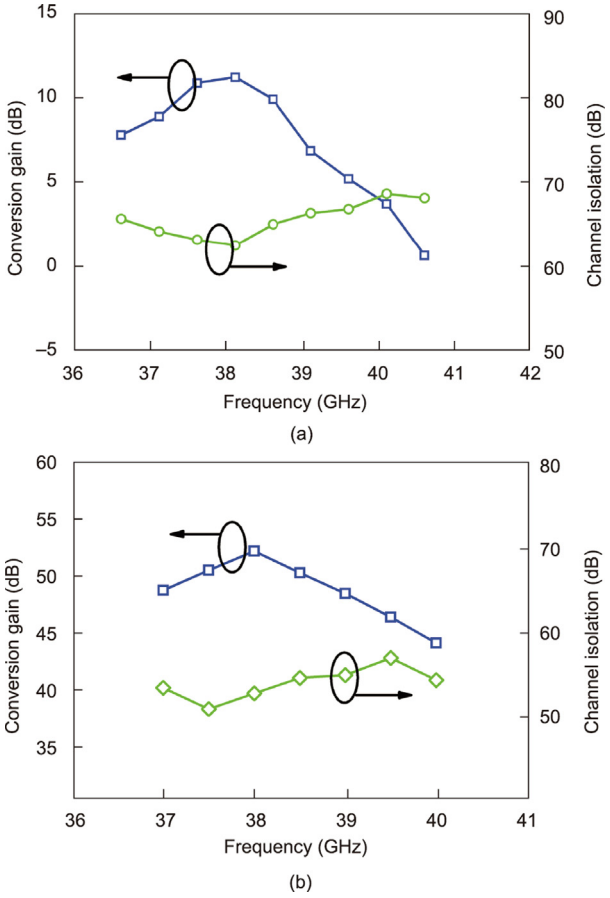


Fig. 19. Measured maximum gain and channel isolation of (a) TX SIP and (b) RX SIP.

of the EM simulation for passive structures may also cause the scale-up of the gain-tuning range. Accordingly, the measured RMS gain errors of the transceiver are worse than the simulated results of the attenuator. As presented in Fig. 20(c), they are 2.8 dB in the TX chip and 1.3 dB in the RX chip.

Fig. 21(a) shows the measured OP_{1dB} and saturated output power (P_{Sat}) of the TX SIP, which are 5.4 and 10.0 dBm at 38.5 GHz, respectively. Compared with the post-layout simulation results of the PA, the tested linearity of the TX deteriorates by approximately 2 dBm. The probable reason is that the chip's operating temperature is higher than the one set in the simulation

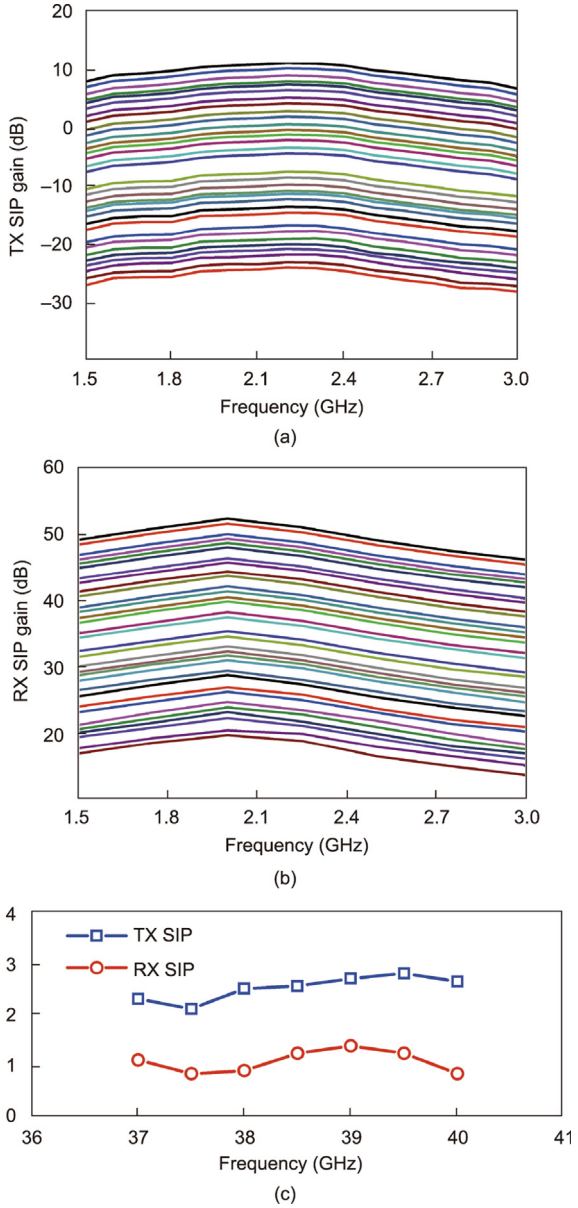


Fig. 20. Measured 32 Gain states. (a) TX SIP; (b) RX SIP; (c) RMS gain errors of the TX SIP and RX SIP.

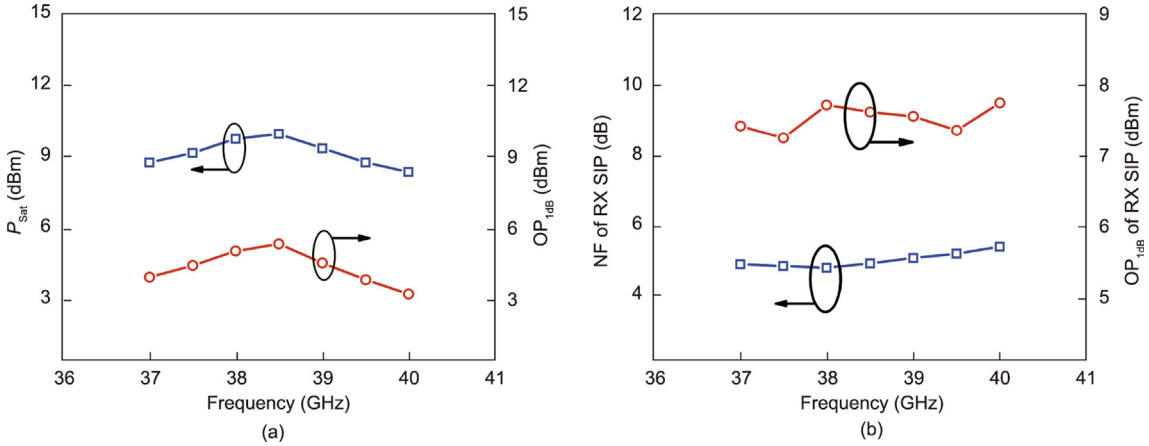


Fig. 21. (a) Measured OP_{1dB} and P_{Sat} of the TX SIP; (b) measured NF and OP_{1dB} of the RX SIP.

environment of the circuit simulation software. The other reason may be that the output matching balun's loss is worse than the EM simulated loss. Within the frequency band of 37–40 GHz, the P_{Sat} of the TX channel is more than 8.4 dBm. The measured OP_{1dB} and NF of the RX SIP are shown in Fig. 21(b). In the maximum gain state, the RX obtains an OP_{1dB} of more than 7.2 dBm and an NF of less than 5.4 dB across 37–40 GHz. When the RX SIP operates in the minimum gain state, the IP_{1dB} is better than −23 dBm. Thus, the RX chip achieves the targeting specifications that were introduced in Section 2. Fig. 22 depict the measured output power and LO leakage power of the TX/RX SIP, which are tested when the IF, LO, and RF frequencies are set to 2.5, 9.0, and 38.5 GHz, respectively. Note that the main spurs in the TX SIP are the 3LO component leaking from the LO to RF ports of the RF mixer and 3LO + LO component generated by the mixture of the RF mixer's LO signal and IF mixer's LO leakage, while those in the RX SIP are the LO component leaking from the LO to IF ports of the IF mixer and 3LO − LO component caused by the mixture of the IF mixer's LO signal and RF mixer's LO leakage. When the LO input power is 5 dBm, the measured spurious suppression of the TX SIP is more than 32 dB (Fig. 22(a)) while that of the RX SIP is more than 22 dB over the targeting frequency band (Fig. 22(b)).

5.2. Wireless communication link measurement

As shown in Fig. 17(c), a single-channel TX-to-RX communication link set up with two antenna modules whose gain is 20 dBi. The TX-to-RX distance is 1 m. A wireless connectivity tester is used to evaluate the EVM performance. The input IF signal is based on IEEE 802.11ac standard, and its bandwidth is 20 MHz, with a carrier of 2.25 GHz (limited by the used equipment). Fig. 23 shows the spectra and constellations of the received signal. Under the peak input signal power of −2.3 dBm for the TX channels, the tested single-channel TX-to-RX EVM and spectral efficiency are 3.72 % and 3.25 $bit \cdot s^{-1} \cdot Hz^{-1}$ with 64-QAM modulation, respectively. With 256-QAM modulation, the demo is also tested and achieves an EVM of 3.76 % and spectral efficiency of 3.90 $bit \cdot s^{-1} \cdot Hz^{-1}$.

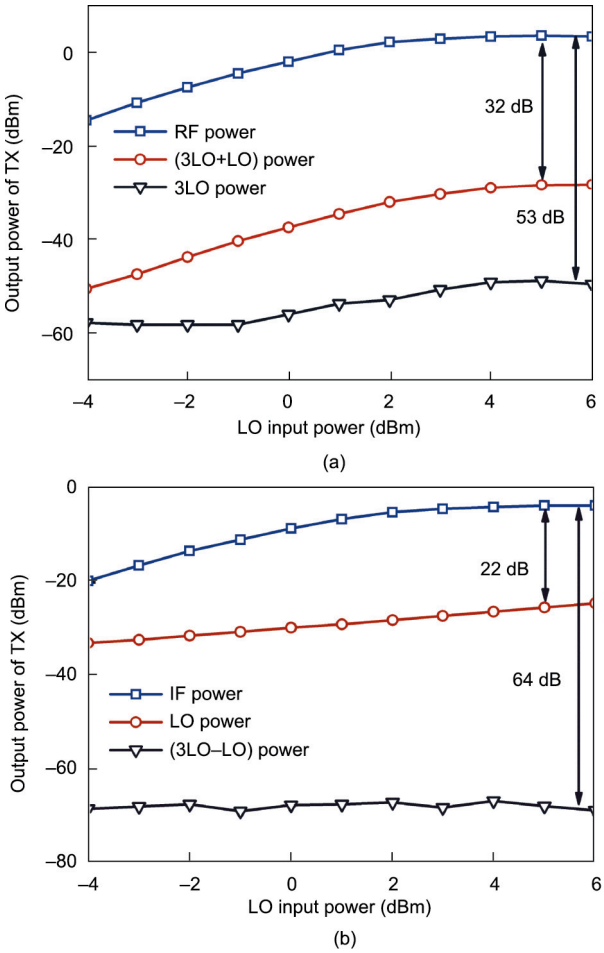


Fig. 22. Tested output power and LO components leakage power. (a) TX SIP; (b) RX SIP.

5.3. 39 GHz multi-beam MIMO prototype

Using the CMOS transceiver chipset, a 39 GHz MIMO prototype is developed [48], as illustrated in Fig. 24. It adopts the dynamic multi-beam architecture shown in Fig. 2(b). The prototype includes four CMOS TX chips and four RX chips; thus, it has eight TX channels and eight RX channels and can support eight independent beams for MIMO operation. The beamformer is designed by a SIW-based Rotman lens and SIW-based slot antenna array with a 20 dBi gain. The measurement results show that each TX channel

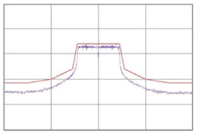
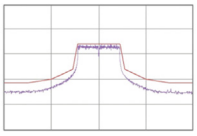
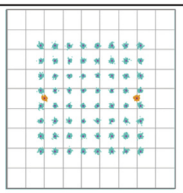
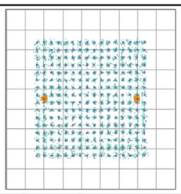
Modulation	64-QAM	256-QAM
Spectrum		
Constellation		
Spectral efficiency	3.25 $bit \cdot s^{-1} \cdot Hz^{-1}$	3.90 $bit \cdot s^{-1} \cdot Hz^{-1}$
TX-to-RX EVM	3.72%	3.76%

Fig. 23. Measured constellation, spectral efficiency, and TX-to-RX EVM. Reproduced from Ref. [37] with permission.

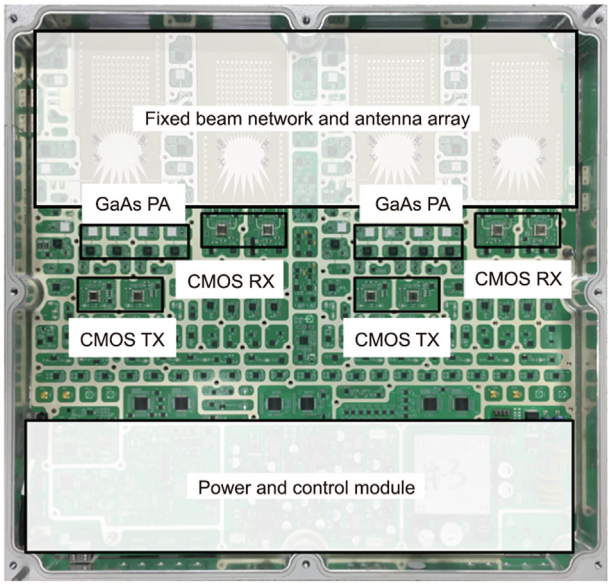


Fig. 24. 39 GHz multi-beam MIMO prototype. Reproduced from Ref. [48] with permission.

achieves an EIRP of more than 52 dBm at the OP_{1dB}, while the NF of the RX channel is less than 7.6 dB across 37–40 GHz.

Online outdoor communication links for one-stream (1S) and two-stream (2S) transmission to single-user equipment (SUE) are demonstrated to evaluate the overall performance of the 39 GHz MIMO system. Fig. 25(a) presents the measurement setup of the outdoor wireless communication. The working distance ranges from 5 to 150 m. This OTA communication link is based on the communication of two sets of access point equipment (APE). The IF signal also adopts IEEE 802.11ac standard and has bandwidth of 80 MHz. The measured downlink throughput of 1S and 2S with different modulation schemes are illustrated in Fig. 25(b). The downlink throughputs of 1S transmission at 5, 50, 100, and 150 m are 185, 150, 130, and 90 megabits per second (Mbps), respectively. To meet the EIRP and linearity requirements for the different working distances, the attenuators are employed to tune the output power and calibrate the gain error of the TX channels and increase the dynamic range of the RX channels. Due to the good EVM performance of the CMOS TX/RX, the proposed MIMO system still can support 16-QAM (modulation and coding scheme 3) modulation at a 150 m distance. In the 2S transmission, the tested throughput of the prototype is almost twice as large as that of the 1S transmission (Fig. 25(b)), and hence the proposed architecture is feasible for multi-beam applications in the mmWave regime.

The overall performances of the front-end chipset are summarized and compared with state-of-the-art 5G mmWave transceivers in Table 3 [10,11,26,33,49,50]. Owing to the above

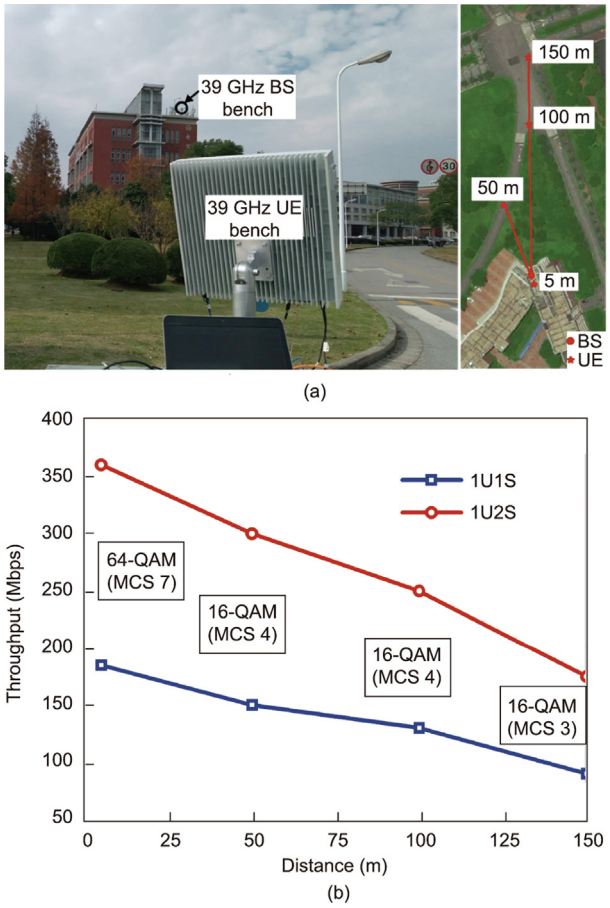


Fig. 25. (a) OTA measurement setup for the 5G MIMO prototype; (b) measured downlink throughputs and modulation scheme over 5–150 m. MCS: modulation and coding scheme; 1U1S: one user with one stream signal; 1U2S: one user with two streams signal. Mbps: megabits per second. Reproduced from Ref. [48] with permission.

Table 3
Performance summary and comparison with the state-of-art 5G mmWave transceivers.

Reference	Process	Architecture	Package	Frequency (GHz)	Channel per chip	MIMO streams	Maximum gain (dB)		Gain range (dB)		TX P_{sat} (dBm)	RX OP_{1dB} (dBm)	RX NF_{min} (dB)	TX-to-RX EVM	P_{DC} (mW)		Chip size (mm^2)	
							TX	RX	TX	RX					TX	RX	TX	RX
Ref. [10]	65 nm CMOS	Phased-array	Flip chip	39	4 TX + RX	1	7.0	3	N/A	N/A	14.0	−9	7.7	3.09 % (64-QAM) 3.16 % (256-QAM)	1500	500	3.00 × 4.00	–
Ref. [11]	65 nm CMOS	Dual polarization + MIMO	Flip chip	28	8 TX + RX	4	20.0	17	N/A	N/A	15.1	N/A	4.2	1.90% (64-QAM) 1.90% (256-QAM)	2000	900	3.00 × 4.00	–
Ref. [26]	65 nm CMOS	Full-connected phased-array	Chip on board	28/37	8 TX + RX	2	43.5/40.0	44/37	22	42	15.5/15.6	14	7.9/8.8	9.60% (16-QAM)	1350	790	2.30 × 5.50	–
Ref. [33]	45 nm RF-SOI	MIMO TX	Flip chip	60	4 TX	4	20.0–35.0	N/A	N/A	N/A	9.1–12.5	N/A	N/A	N/A	880	N/A	3.20 × 4.90	–
Ref. [49]	65 nm CMOS	MIMO + digital beamforming	Chip on board	28	4 RX	4	N/A	16	N/A	N/A	N/A	N/A	6.0	N/A	N/A	248	N/A	1.95 × 2.95
Ref. [50]	180 nm SiGe BiCMOS	Dual Polarization + phased-array	Flip chip	28	8 TX + RX	2	21.0	18	25	25	12.0[a]	−4	4.8	4.80% (64-QAM)	1760	1200	4.80 × 4.80	–
This work	65 nm CMOS	Multi-beam MIMO	LTCC	39	2TX, 2RX	2	11.1	52	33	33	10.0	7.7	5.4	3.72 % (64-QAM) 3.76 % (256-QAM)	440	370	2.80 × 2.80	2.40 × 2.80

P_{DC}: DC power consumption; BiCMOS: bipolar complementary metal-oxide semiconductor; N/A: no answer; SOI: silicon-on-insulator.
[a] OP_{1dB}.

techniques, the transceiver chipset attains the largest gain range of 33 dB and excellent NF and linearity with comparable power consumption, compared with the other works in Table 3.

6. Conclusions

In this article, a 39 GHz transceiver chipset is proposed and demonstrated for 5G mmWave applications. Each TX/RX chip integrates two variable-gain frequency-conversion channels and can support two simultaneous independent beams. Several layout considerations and circuit techniques are introduced to improve the overall performance of the mmWave front-end system. Furthermore, a TX and RX shared LTCC package with excellent RF performance is developed for the 39 GHz chipset. The TX-to-RX wireless communication link measurement characteristics show that the proposed 39 GHz transceiver chipset can support even 256-QAM modulation transmission. A 39 GHz multi-beam MIMO prototype is also developed based on the CMOS transceiver chipset. OTA communication testing indicates that the prototype successfully achieves MIMO operation over 5–150 m distance. Therefore, the proposed CMOS transceiver and dynamic multi-beam architecture are feasible for mmWave MIMO applications. This article provides a potential solution for 5G mmWave communication.

Acknowledgments

This work was supported in part by National Natural Science Foundation of China (62171102 and 61931007), and in part by National Key Research and Development Program of China (2020YFB1805003).

Compliance with ethics guidelines

Yiming Yu, Zhilin Chen, Chenxi Zhao, Huihua, Liu, Yunqiu Wu, Wen-Yan Yin, and Kai Kang declare that they have no conflict of interest or financial conflicts to disclose.

References

[1] Carlson EK. What will 5G bring? Engineering 2020;6(7):725–7.
[2] Sadhu B, Tousi Y, Hallin J, Sahl S, Reynolds SK, Renström Ö, et al. A 28 GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications. IEEE J Solid State Circuits 2017;52(12):3373–91.
[3] Kibaroglu K, Sayginer M, Rebeiz GM. A low-cost scalable 32-element 28 GHz phased array transceiver for 5G communication links based on a 2 × 2 beamformer flip-chip unit cell. IEEE J Solid State Circuits 2018;53(5):1260–74.
[4] Chen CN, Lin YH, Hung LC, Tang TC, Chao WP, Chen CY, et al. 38 GHz phased array transmitter and receiver based on scalable phased array modules with endfire antenna arrays for 5G MMW data links. IEEE Trans Microw Theory Tech 2021;69(1):980–99.
[5] Yang B, Yu Z, Lan J, Zhang R, Zhou J, Hong W. Digital beamforming-based massive MIMO transceiver for 5G millimeter-wave communications. IEEE Trans Microw Theory Tech 2018;66(7):3403–18.
[6] Mondal S, Singh R, Hussein AI, Paramesh J. A 25–30 GHz fully-connected hybrid beamforming receiver for MIMO communication. IEEE J Solid State Circuits 2018;53(5):1275–87.
[7] Yeh YS, Floyd BA. Multibeam phased-arrays using dual-vector distributed beamforming: architecture overview and 28 GHz transceiver prototypes. IEEE Trans Circuits Syst I Regul Pap 2020;67(12):5496–509.
[8] Vook FW, Ghosh A, Thomas TA. MIMO and beamforming solutions for 5G technology. In: Proceedings of IEEE MTT-S International Microwave Symposium (IMS2014); 2014 Jun 1–6; Tampa, FL, USA; 2014.
[9] Ayach OE, Rajagopal S, Abu-Surra S, Pi Z, Heath RW. Spatially sparse precoding in millimeter wave MIMO systems. IEEE Trans Wirel Commun 2014;13(3):1499–513.
[10] Wang Y, Wu R, Pang J, You D, Fadila AA, Saengchan R, et al. A 39 GHz 64-element phased-array transceiver with built-in phase and amplitude calibrations for large-array 5G NR in 65-nm CMOS. IEEE J Solid State Circuits 2020;55(5):1249–69.
[11] Pang J, Li Z, Kubozoe R, Luo X, Wu R, Wang Y, et al. A 28 GHz CMOS phased-array beamformer utilizing neutralized bi-directional technique supporting dual-polarized MIMO for 5G NR. IEEE J Solid State Circuits 2020;55(9):2371–86.
[12] Yin Y, Ustundag B, Kibaroglu K, Sayginer M, Rebeiz GM. Wideband 23.5–29.5 GHz phased arrays for multistandard 5G applications and carrier aggregation. IEEE Trans Microw Theory Tech 2021;69(1):235–47.
[13] Dunworth J, Ku BH, Ou YC, Lu D, Mouat P, Homayoun A, et al. 28 GHz phased array transceiver in 28 nm bulk CMOS for 5G prototype user equipment and base stations. In: Proceedings of IEEE/MTT-S International Microwave Symposium—IMS; 2018 Jun 10–15; Philadelphia, PA, USA;2018.
[14] Park H-C, Kang D, Lee SM, et al. A 39GHz-band CMOS 16-channel phased-array transceiver IC with a companion dual-stream IF transceiver IC for 5G NR base-station applications. In: Proceedings of IEEE/MTT-S International Microwave Symposium—IMS; 2018 Jun 10–15; Philadelphia, PA, USA; 2018.
[15] Yu Y, Zhu J, Zong Z, Tang P, Liu H, Zhao C, et al. A 21-to-41 GHz high-gain low noise amplifier with triple-coupled technique for multiband wireless applications. IEEE Trans Circuits Syst II Express Briefs 2021;68(6):1857–61.
[16] Bailleul PK. A new era in elemental digital beamforming for spaceborne communications phased arrays. Proc IEEE 2016;104(3):623–32.
[17] Ma S, Wu T, Zhang J, Ren JA. 5G wireless event-driven sensor chip for online power-line disturbances detecting network in 0.25 μm GaAs process. IEEE Trans Ind Electron 2021;68(6):5271–80.
[18] Zhu W, Wang J, Lv W, Zhang X, Liao B, Zhu Y, et al. A 24–28 GHz power and area efficient 4-element phased-array transceiver front-end with 21.1%/16.6% transmitter peak/OP_{1dB} PAE supporting 2.4 Gb/s in 256-QAM for 5G communications. In: Proceedings of IEEE Radio Frequency Integrated Circuits Symposium (RFIC); 2020 Aug 4–6; Los Angeles, CA, USA; 2020.
[19] Yu C, Jing J, Shao H, Jiang ZH, Yan P, Zhu XW, et al. Full-angle digital predistortion of 5G millimeter-wave massive MIMO transmitters. IEEE Trans Microw Theory Tech 2019;67(7):2847–60.
[20] Hong Z, Schonherr S, Chauhan V, Floyd B. Free-space phased-array characterization and calibration using code-modulated embedded test. In: Proceedings of IEEE MTT-S International Microwave Symposium (IMS); 2019 Jun 2–7; Boston, MA, USA; 2019.
[21] Chan HC, Kuo YJ, Chen WY, Chang SF. A Ku-band CMOS build-in-self-test chip based on phasor-sum detection method for RF beamforming transceivers. In: Proceedings of IEEE MTT-S International Microwave Symposium (IMS); 2017 Jun 4–9; Honolulu, HI, USA; 2017.
[22] Chen D, Zhang X, Zhang L, Chen L, Sun S, Liu Y, et al. A Ku-band 8-element phased array transmitter with built-in-self-test capability. In: Proceedings of IEEE/MTT-S International Microwave Symposium—IMS; 2018 Jun 10–15; Philadelphia, PA, USA; 2018.
[23] Sowlati T, Sarkar S, Perumana BG, Chan WL, Toda AP, Afshar B, et al. A 60 GHz 144-element phased-array transceiver for backhaul application. IEEE J Solid State Circuits 2018;53(12):3640–59.
[24] Nafe A, Kibaroglu K, Sayginer M, Rebeiz GM. An *insitu* self-test and self-calibration technique utilizing antenna mutual coupling for 5G multi-beam TRX phased arrays. In: Proceedings of IEEE MTT-S International Microwave Symposium (IMS); 2910 Jun 2–7; Boston, MA, USA; 2019.
[25] Mondal S, Paramesh J. A reconfigurable 28/37 GHz MMSE adaptive hybrid-beamforming receiver for carrier aggregation and multistandard MIMO communication. IEEE J Solid State Circuits 2019;54(5):1391–406.
[26] Mondal SL, Carley R, Paramesh J. A 28/37 GHz scalable, reconfigurable multi-layer hybrid/digital MIMO transceiver for TDD/FDD and full-duplex communication. In: Proceedings of A 28/37GHz scalable, reconfigurable multi-layer hybrid/digital MIMO transceiver for TDD/FDD and full-duplex communication; 202 Feb 16–20; San Francisco, CA, USA; 2020.
[27] Natarajan A, Valdes-Garcia A, Sadhu B, Reynolds SK, Parker BD. W-band dual-polarization phased-array transceiver front-end in SiGe BiCMOS. IEEE J Solid State Circuits 2015;63(6):1989–2002.
[28] Aljuhani AH, Kanar T, Zihir S, Rebeiz GM. A scalable dual-polarized 256-element Ku-band phased-array SATCOM receiver with ±70° beam scanning. In: Proceedings of IEEE/MTT-S International Microwave Symposium—IMS; 2018 Jun 10–15; Philadelphia, PA, USA; 2018.
[29] Roh W, Seol JY, Park J, Lee B, Lee J, Kim Y, et al. Millimeter-wave beamforming as an enabling technology for 5G cellular communications: theoretical feasibility and prototype results. IEEE Commun Mag 2014;52(2):106–13.
[30] Brady J, Hogan J, Sayeed A. Multi-beam MIMO prototype for real-time multiuser communication at 28 GHz. In: Proceedings of IEEE Globecom Workshops (GC Wkshps); 2016 Dec 4–8; Washington, DC, USA; 2016.
[31] Duarte VC, Prata JG, Ribeiro C, Nogueira RN, Winzer G, Zimmermann L, et al. Integrated photonic true-time delay beamformer for a Ka-band phased array antenna receiver. In: Proceedings of Optical Fiber Communication Conference ; 2018 Mar 11–15; San Diego, CA, USA; 2018.
[32] Huang MY, Chen YW, Shiu RK, Wang H, Chang GK. A bi-directional multi-band, multi-beam mm-wave beamformer for 5G fiber wireless access networks. J Lightwave Technol 2021;39(4):1116–24.
[33] Binaie A, Ahasan S, Dascurcu A, Dastjerdi MB, Garg R, Johnson M, et al. A scalable 60 GHz 4-element MIMO transmitter with a frequency-domain-multiplexing single-wire interface and harmonic-rejection-based de-multiplexing. In: Proceedings of IEEE Radio Frequency Integrated Circuits Symposium (RFIC); 2020 Aug 4–6; Los Angeles, CA, USA; 2020.

[34] Xu JX, Zhang XY. Single- and dual-band LTCC filtering switch with high isolation based on coupling control. IEEE Trans Ind Electron 2017;64(4):3137–46.
[35] Zhang Y. Antenna-in-package (AiP) technology. Engineering 2022;11:18–20.
[36] Kam DG, Liu D, Natarajan A, Reynolds S, Chen HC, Floyd BA. LTCC packages with embedded phased-array antennas for 60 GHz communications. IEEE Microw Wirel Compon Lett 2011;21(3):142–4.
[37] Chen Z, Jiang Z, Liu Z, Cheng Y, Zhang L, Cheng D, et al. A 256-QAM 39 GHz dual-channel transceiver chipset with LTCC package for 5G communication in 65 nm CMOS. In: Proceedings of IEEE/MTT-S International Microwave Symposium—IMS; 2018 Jun 10–15; Philadelphia, PA, USA; 2018.
[38] Chen P, Hong W, Kuai Z, Xu J, Wang H, Chen J, et al. A multibeam antenna based on substrate integrated waveguide technology for MIMO wireless communications. IEEE Trans Antennas Propag 2009;57(6):1813–21.
[39] Cheng YJ, Hong W, Wu K, Kuai ZQ, Yu C, Chen JX, et al. Substrate integrated waveguide (SIW) Rotman lens and its Ka-band multibeam array antenna applications. IEEE Trans Antennas Propag 2008;56(8):2504–13.
[40] Yu Y, Cao J, Zong Z, Tang P, Yi K, Zhao C, et al. A 68.5–90 GHz high-gain power amplifier with capacitive stability enhancement technique in 0.13 μm SiGe BiCMOS. IEEE Trans Microw Theory Tech 2020;68(12):5359–70.
[41] Razavi B. RF Microelectronics. 2nd ed. New Jersey: Prentice Hall Press; 2011.
[42] Wu R, Minami R, Tsukui Y, Kawai S, Seo Y, Sato S, et al. 64-QAM 60 GHz CMOS transceivers for IEEE 802.11ad/ay. IEEE J Solid State Circuits 2018;52(11):2871–91.
[43] Chen Z, Liu H, Liu Z, Jiang Z, Yu Z, Wu Y, et al. A 62–85 GHz high linearity up conversion mixer with 18 GHz IF bandwidth. IEEE Microw Compon Lett 2019;29(3):219–21.
[44] Zhao C, Zeng X, Zhang L, Liu H, Yu Y, Wu Y, et al. A 37–40 GHz low-phase imbalance CMOS attenuator with tail-capacitor compensation technique. IEEE Trans Circuits Syst I Regul Pap 2020;67(10):3400–9.
[45] Yu Y, Liu H, Wu Y, Kang K. A 54.4–90 GHz low-noise amplifier in 65 nm CMOS. IEEE J Solid State Circuits 2017;52(11):2892–904.
[46] Zhang J, Liu H, Zhao C, Kang K. A 22.8-to-43.2 GHz tuning-less injection-locked frequency tripler using injection-current boosting with 76.4% locking range for multiband 5G applications. In: Proceedings of IEEE International Solid-State Circuits Conference—(ISSCC); 2018 Feb 11–15; San Francisco, CA, USA; 2018.
[47] Lee YC, Park CS. A fully embedded 60 GHz novel BPF for LTCC system-in-package applications. IEEE Trans Adv Packag 2006;29(4):804–9.
[48] Li X, Chen Z, Sun S, Zhao C, Liu H, Wu Y, et al. A 39 GHz MIMO transceiver based on dynamic multi-beam architecture for 5G communication with 150 meter coverage. In: Proceedings of IEEE/MTT-S International Microwave Symposium—IMS; 2018 Jun 10–15; Philadelphia, PA, USA; 2018.
[49] Johnson M, Dascuru A, Zhan K, Galioglu A, Adepu N, Jain S, et al. A 4-element 28 GHz millimeter-wave MIMO array with single-wire interface using code-domain multiplexing in 65 nm CMOS. In: Proceedings of IEEE Radio Frequency Integrated Circuits Symposium (RFIC); 2019 Jun 2–4; Boston, MA, USA; 2019.
[50] Kibaroglu K, Sayginer M, Nafe A, Rebeiz GM. A dual-polarized dual-beam 28 GHz beamformer chip demonstrating a 24 Gbps 64-QAM 2 × 2 MIMO link. In: Proceedings of IEEE Radio Frequency Integrated Circuits Symposium (RFIC); 2018 Jun 10–12; Philadelphia, PA, USA; 2018.