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News & Highlights

Nanosheet Chips Poised to Rescue Moore's Law

Robert Pollie

Senior Technology Writer

The semiconductor industry reached a major milestone recently when IBM Research, the research and development division of International Business Machines Corporation (IBM), demonstrated what it billed as "the world's first 2 nm chip" in May 2021 (Fig. 1) [1]. The test chip uses a breakthrough technology called stacked nanosheets to achieve new levels of transistor density (transistors per square millimeter), paving the way for faster, more energy-efficient semiconductors.

"Nanosheet technology provides new impetus for Moore's Law," said Jesús del Alamo, professor of electrical engineering at the Massachusetts Institute of Technology (MIT) in Cambridge, MA, USA. "We should continue to expect dramatic improvements in chip technology for quite a few years to come."

That is welcome news, since Moore's Law has been an engine of technological progress over the last half-century, fueling a steady procession of smarter, more affordable, and more efficient digital products [2]. Del Alamo points out that a brighter future for Moore's Law may also bolster US government support for programs aimed at strengthening American chip production and competitiveness [3]. "In the United States, we are discussing big investments to regain leadership in advanced chip technology," he said. "And you only want to do that if you can sustain the leadership through continued long-term improvements."

In recent years some observers had predicted that Moore's Law—which posits a doubling of chip densities every few years—was no longer sustainable. The prevailing transistor architecture, the fin field-effect transistor (FinFET), was running up against fundamental physical limits and could not shrink much further [4]. Nanosheets overcome these barriers, enabling greater miniaturization and higher density. Specifically, nanosheets use a "gate-all-around" (GAA) design to tightly control current and stanch the electrical leakage that plagues FinFETs at small scales.

Chip transistors function as tiny electrical switches, using metallic gates to toggle the flow of current on and off. In FinFETs, which have been the reigning transistor architecture for the last decade, the current-carrying channel consists of a thin vertical fin made of silicon, bordered on three sides by the gate. The problem is that as the transistor dimensions get smaller, FinFET gates are no longer able to completely shut off the current. Electrons continue to seep through the channel even when the transistor is in the "off" state, wasting power and generating heat [5].

A nanosheet transistor replaces the FinFET's fin-shaped channel with a stack of horizontal silicon sheets, each completely surrounded by gate materials (Fig. 2). This superior gate coverage (four sides as opposed to three) provides better electrostatic control and minimizes leakage in the off state.

Nanosheets also offer greater design flexibility, letting chipmakers fine tune trade-offs between performance and power consumption by tweaking the width of the sheets (wider sheets allow more current and faster switching, while narrower sheets constrict current and reduce energy usage). In FinFETs, by contrast, the dimensions of the fin are fixed, so designers are limited to making coarse-grained adjustments by varying the number of fins [6].

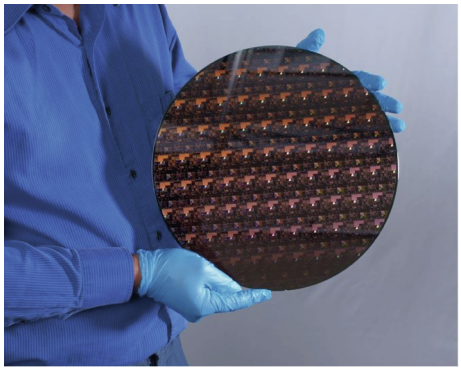

Fig. 1. This silicon wafer fabricated at IBM Research in Albany, NY, USA, contains hundreds of 2 nm chips. Credit: IBM Research, with permission.

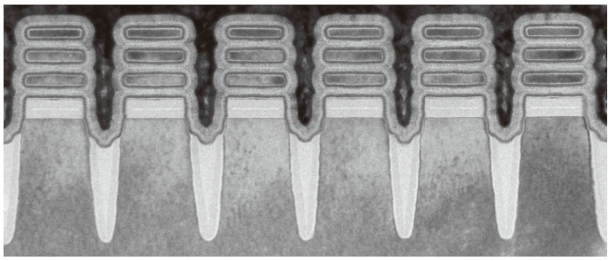

Fig. 2. A transmission electron micrograph shows a row of IBM's 2 nm stacked nanosheet transistors. Each transistor has three nanosheets surrounded by gate materials. Credit: IBM Research, with permission.

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Nanosheets have been in development for years. IBM Research showed the technology's feasibility in 2017, demonstrating working nanosheet transistors that, according to the company, could scale to 5 nm [7]. IBM's latest nanosheet chip takes things significantly further. At 2 nm, it is several generations denser than today's leading-edge 7 nm chips, and well beyond the limits of FinFETs, which are impractical at scales below 3 nm. Note that "7 nm," "5 nm," and "3 nm" do not refer to exact measurements of chip features. Rather, they are industry shorthand for semiconductor process generations ("nodes"), with each successive node delivering roughly twice the transistor density of the prior one.

IBM claims its 2 nm nanosheet technology will enable 50 billion transistors to be squeezed onto a chip measuring 150 mm^2 (about the size of a fingernail), and that it will deliver 45% higher performance or 75% lower power consumption compared to cutting-edge 7 nm chips [8].

"We expect the 2 nm technology to go into production by the end of 2024," said Mukesh Kahre, vice president of Cloud at IBM Research. IBM will not be producing the chips itself—the company stopped making semiconductors in 2014 [9]—but will work with manufacturing partners to commercialize the technology. In creating a functional 2 nm test chip, "IBM has already done the hardest part," said Dan Hutcheson, chief executive officer of VLSI Research, a semiconductor market research firm in San Jose, CA, USA. "Now the challenge is getting high yields and reliably high volumes."

Chips based on IBM's nanosheet technology will likely serve a wide range of systems, from handheld mobile devices to high-end servers, Kahre said. Performance-optimized 2 nm chips could give a big lift to processing-intensive applications such as artificial intelligence, autonomous vehicles, and machine learning, while low-power versions could extend battery life in mobile systems and reduce the carbon footprint of data centers. IBM itself will likely be among the first customers for the new chips, using them in products such as its Power line of enterprise servers [10].

IBM is not the only company making the move to nanosheets; all the top three semiconductor manufacturers have put the technology on their roadmaps. Samsung plans to deploy its version of nanosheet transistors, called Multi-Bridge Channel FET (MBCFET), in 3 nm chips as soon as 2022 [6], while Intel is slated to introduce its "RibbonFET" nanosheet chips by 2024 [11]. Taiwan Semiconductor Manufacturing Company Ltd. (TSMC) will reportedly stick with FinFETs down to 3 nm and then transition to nanosheets at 2 nm [12].

How far can chipmakers ride the nanosheet wave? Hutcheson believes the technology's impact will be long-lasting because it opens a new dimension in chip design. "Now you can go vertical," he said. "Not only can you stack nanosheets to create individual transistors, but you can stack transistors on top of each other." That is because, in nanosheet transistors, the channels and other elements are layered on top of the silicon substrate. Adding more transistors just means applying more layers, like adding another floor on top of a building. In FinFETs, on the other hand, the fin-shaped channel is carved out of the silicon substrate itself, so transistors are confined to the "ground floor" with no ability to add more levels.

Intel has already demonstrated multi-transistor stacking, using nanosheet technology to piggyback an N-channel metal oxide semiconductor (NMOS) transistor on top of a P-channel metal oxide semiconductor (PMOS) transistor [13]. In conventional designs, these two types of transistors, which together make up a complementary metal oxide semiconductor (CMOS) circuit (a basic building block of chips), are laid out side-by-side. By stacking them, designers can slice the footprint in half. This space-saving maneuver—building upwards, not outwards—has potentially profound implications for semiconductor technology.

"You can still get density increases even when you are not shrinking transistors," said Hutcheson. "This is a game-changer. It provides a way to continue increasing transistor counts even after you run into size limitations in the core technology. It is a whole new way to improve density in logic semiconductors. That is why I think we can push out Moore's Law 10 to 20 years."

Moore's Law may have gotten a reprieve, but density improvements cannot go on forever. Circuit designers can only pack so many transistors into a finite space. Undaunted, researchers are exploring other ways to enhance chip performance and conserve power. Del Alamo and his group at MIT, for example, are exploring the possibility of replacing the silicon traditionally used in transistor channels with new materials such as indium gallium arsenide (InGaAs). Such compounds "allow electrons to travel faster, and everything else being equal, we can get more current and higher performance; or conversely, we can reduce voltage and cut power consumption," he said. "But as you can imagine there are many new challenges that will emerge."

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